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Active RF Cavity and Applications

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Active RF cavity amplifier (ARFCA) is a solid state device (SSD) based amplifier which uses the cavity simultaneously as the combiner, the matching transformer and the heat sink. AS prototype device was developed using six Motorola MFR/6030 transistors or equivalent operating over 1.6 - 1.7 GHz. The device as given by the Motorola data book has a nominal (below saturation) output power gain at 7.5dB min and 7.7 dB typical with collector efficiency at 40% minimum and 45% typical. The prototype ARFCA has a measured gain of 8.4 dB with efficiency 45.4% at 198.2 W output power. The model can be assembled by hand tools and requires no soldering. It uses no discrete passive electronic components except the few capacitors associated with the bias power supply.

A high power model at 1.2 kW and 915 MHz is being developed, aiming for applications in industrial and chemical processing. Because of its high efficiency and reliability and low cost manufacturing, ARFCA promises to become a desirable rf source in many high power high frequency applications.

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SUMMARY

In the present state of electronics technology, transistors, with few other devices often known collectively as solid state devices (SSDs) have replaced vacuum electronic devices (vacuum tubes) and effected a revolution in this industry. One does not need to be an expert in the electronics field to realize the extent of the impact that this revolution has caused. However in the applications and systems where both high power and high frequency are required, the SSD technology has not yet been able to make any effective inroads. The attempt to combine low power SSDs to form high power devices has been less successful. The process is complex and requires high labor skill, and is not amenable to large scale mass production. The product efficiency deteriorates rapidly as the number of discrete SSDs needed is increased. The final product is inevitably one of high cost and poor performance. To date in areas such as over the air broadcasting, various radar systems, industrial heating and processing etc., tubes ¹ remain the dominant technology to provide the high frequency high power required.

The active rf cavity amplifier (ARFCA) technology is based on the patented concept of active resonant cavity which enables the integration of a large number of low power SSDs into the conductive cavity wall to form a monolithic high power structure efficiently. It can be mass-produced with low level facilities and low skill labor and is thus extremely cost-competitive. With the inherent advantages of a SSD based technology, such as high reliability, small size, light weight low voltage power supply etc., it should be able to quickly acquire a significant share of the market which is presently dominated by tubes. It should also be possible to find new applications which are presently closed because of the limitations of the current technologies.

The program, as sponsored by BMDO/SDIO, administered by DSWA (formerly DNA), in two successive SBIR contracts, resulted in the successful development of a prototype which shows all its various features leading toward a product of high performance and low cost; and of interest to both military and non-military applications. Various commercialization avenues are being developed including seeking synergistic business relations with other corporations and in-house manufacturing using low-skill labor force and low-level facility.

¹Tubes used in high frequency applications are known generically as microwave tubes which are much more complex than the tubes used for low frequency applications. They require precision fabrication of its various interior parts and generally require a magnetic structure. There have been only a handful of companies associated with this technology. They are regarded as part of the defense industry and are going through the similar restructuring process.

CONVERSION TABLE

Multiply	by	to Get
To Get	by	Divide

angstrom	1.000 000 X E -10	meters (m)
degree Fahrenheit	$t_c = .5555(t_{f}^0 32)$	degree Celsius
electron volt	1.602 19 X e -19	joule (J)
erg	1.000 000 X E -7	joule (J)
erg/second	1.000 000 X E -7	watt (W)
foot	3.048 000 X E -1	meter (m)
inch	2.540 000 X E -2	meter (m)

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SECTION 1 INTRODUCTION

Active RF Cavity (ARFC) is an RF engineering concept which enables the integration of a large number of lower power rf solid state devices (SSDs) into a high power structure. When the combined high power is piped out to an RF load, the structure becomes a high power amplifier/source and is termed active rf cavity amplifier (ARFCA). A US patent² on this invention has been granted to the Polytechnic University and an exclusive license agreement has been executed with Aria Microwave Systems Inc. for the development and commercialization of this technology.

The funding of the research and development effort leading to a prototype AFRCA was obtained from a Small Business Innovative Research Program grant (SBIR, Phase I³ and Phase II) from the Ballistic Missile Defense Organization (BMDO) and the program was administered by the Defense Special Weapons Agency (DSWA), formerly Defense Nuclear Agency (DNA) via two successive contracts.

The present report constitutes the final report of the Phase II program, summarizing the accomplishments, efforts and out look of the technology. The main goal of the program, the construction of a prototype ARFCA model for proof of principle, has been achieved with results beyond expectations. The prototype, operating over 1.6 - 1.7 GHz., consists of six Motorola MRF 16030 devices at 30W nominal power each. The maximum output power at 198.2 W for the amplifier was achieved well below the saturation of the devices. The system gain at 8.4 dB and the overall efficiency output (output rf power divided by the dc power) at 45.4% -47.7% were higher than the typical values given in the Motorola Data Book for the individual MRF 16030 transistors. This shows that the cavity circuitry for ARFCA is more efficient than the manufacturer's own test circuit fixture. The model includes no discrete passive electronic components in the combining system and can be assembled with hand tools and without soldering. This points toward a product which is of high performance and reliability, and is amenable to low cost manufacturing, by low skill level labor and at a low level facility. This suggests that ARFCA can make inroads into the market areas traditionally dominated by tubes, as well as, in applications which is presently closed because of the limitations of current technologies.

A high power production prototype at 915 MHz and 1 kW is being developed, aiming for the industrial heating material processing market. The model consists of 20 transistors at 60W each. Experimental results have shown that the AFRCA principle holds equally well with a 20 device model. The present effort is concentrated on the suppression of some instabilities inherent in the transistors used. We are working with good technical assistance from device manufactures and also simultaneously exploring alternatives solutions with other suppliers. We expect successful resolution in the near future.

² B.R. Cheo, US Patent # 5,497,050 "Active RF Cavity Including a Plurity of Solid State Transistors"; March 5, 1996

³ B.R. Cheo, Meng-Kun Ke, J. Shmoys and F. Cassara, "Active RF Cavity and Applications" Phase I Final Report, Contract DNA001-93-0097; 1994

Throughout the past two years, we have been pursuing various commercialization plans. Initially we devoted all our effort in this endeavor by looking for the various partnering modalities with established companies. This effort continues presently as synergistic relations are being sought in several application areas:

- Radar systems: Air traffic control, weather, as well as any appropriate military systems.
- Plasma lighting: Sulfur lighting in particular.
- FM broadcasting: terrestrial broadcasting require kW level transmitters.
- Chemical plants and other industrial applications.

Since the early spring of 1996, we began to realize that we may be able to expand the commercialization into manufacturing. The required resources is minimal and profit is high. This effort can begin as soon as the instability problem of the 915 MHz model is resolved.

A business plan is being prepared.

Section 2 of this report gives the theoretical background of ARFCA and discussions on various technical issues pertaining to the performance of the amplifier. Section 3 describes a practical design showing various components required. Section 4 describes the 1.6 - 1.7 GHz model prototype. The 915 MHz 1 kW pre-production prototype and various technical issues are discussed in Section 5. Section 6 describes the commercialization effort. The final section describes various independent studies pertinent to the active rf cavity concept and applications.

SECTION 2 ARFCA PRINCIPLE - FUNDAMENTAL THEORY

2.1 BASIC PRINCIPLE.

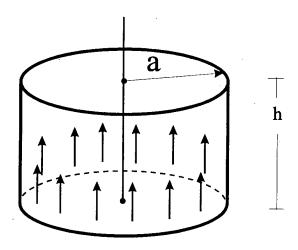


Figure 2-1. Cylindrical cavity.

Consider a cylindrical cavity with radius **a** and height **h** as shown in Figure 2-1. With respect to a cylindrical coordinate system (r,ϕ,z) , the electromagnetic field of the resonant TM_{010} mode is given by 4

$$\vec{E} = \vec{a}_z E_0 J_0(kr)$$

$$\vec{H} = \vec{a}_\phi \sqrt{\frac{\varepsilon}{\mu}} E_0 J_1(kr)$$
(2.1)

where

 \vec{a}_z and \vec{a}_{ϕ} are unit vectors

 ϵ and μ are permittivity and permeability of the medium filling the cavity

 E_0 is an arbitrary amplitude

 $J_{o}(x)$ and $J_{1}(x)$ are respectively the zeroth and the first order Bessel Functions.

⁴ S. Ramo, J.R. Whinnery and T Van Duzer, "Fields and Waves in Communication Electronics", Ch. 10, John Wiley and Sons, Inc., New York.London.Sydney, 1965

At resonance, ka = 2.405 the first zero of $J_0(x)$.

$$k = \omega \sqrt{\mu \varepsilon} = \omega / c$$

The resonant frequency $f_o = 2.405c/2\pi a = 1.148x10^{10}/a$ where a is radius in cm.

The surface current J_s on the cavity wall is given by

$$\vec{J}_s = -\vec{a}_r \times \vec{H} = -\vec{a}_z j \sqrt{\frac{\varepsilon}{\mu}} E_0 J_1(ka)$$
 (2.2)

as shown.

The energy stored in the cavity is equal to the sum of the instantaneous electric and magnetic field energies, and is a constant in time proportional to $|E_o|^2$, if the system is lossless. If loss, including piping out the energy via a waveguide or a transmission line, is present, the energy stored and thus the field amplitude $|E_o|$ shall decrease exponentially. To maintain the amplitude, external power source must be used to make up this loss.

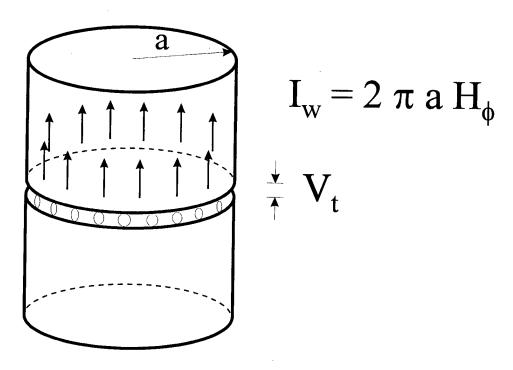


Figure 2-2. Cylindrical cavity with slit.

Consider conceptually the same cavity as in Figure 2-1 with a slit cut into the side wall, and a set of voltage generators with amplitude V_t^5 connected across the gap as shown in Figure 2-2. When the cavity loss is present, V_t must be turned on to supply the power lost from the cavity, maintaining a steady state.

$$\frac{1}{2}V_tI_w = P_c \tag{2.3}$$

Where I_w = $2\pi a~J_s$ = $2\pi a~H_\phi$, the total wall current; P_c is the total cavity power loss.

The interesting fact of this simple background is that the impedance seen across the gap

$$Z_g = \frac{V_t}{I_w} \tag{2.4}$$

is compatible with a large number of transistors connected in parallel. The cavity now serves simultaneously as the power combiner, the matching transformer and the heat sink when the transistors are mounted in the wall. This is the fundamental principle of the active cavity concept, a resonant cavity with active elements imbedded within the cavity wall. The above can also be extended to a high order TM_{omo} modes.

2.2 EQUIVALENT CIRCUIT.

An equivalent circuit can be developed for the structure shown in Figure 2-2. We look for the input impedance Z_g seen across the gap near the resonant frequency. From basic network theory, it is known that the resonant frequency should be a simple zero. Thus near the resonant frequency, Z_g can be represented by a simple RLC circuit as shown in Figure 2-3.

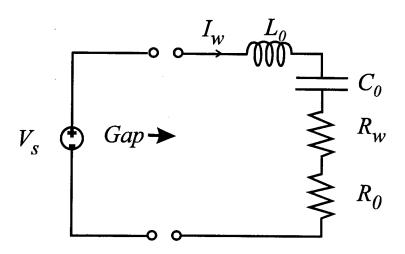


Figure 2-3. Equivalent circuit.

⁵Throughout this report, peak value of an ac quantify is used in the phasor notation, i.e. $v(t) = \text{Re } V e^{j\omega t} = V_o \cos(\omega t + \theta)$, $V = V_o e^{j\theta}$

Where:

$$\frac{1}{2}I_w^2 R_w = P_w = wall \ loss$$

$$\frac{1}{2}I_w^2 R_0 = P_{load}$$
(2.5)

 P_{load} can either be the power output when the power is piped out or that to some other output power absorbing agent with in the cavity, e.g. food in a microwave oven.

L₀ is obtained from

$$\frac{1}{2}I_{w}^{2}L_{0} = \text{total energy stored in the cavity}$$
 (2.6)

 C_0 is given by the resonant frequency $\omega_o^2 = 1/L_0C_0$

$$R_w = R_s \left(\frac{h}{2\pi a} + \frac{1}{2\pi} \right) \tag{2.6}$$

where R_s is the surface resistance.

$$L_0 = \frac{\mu h}{4\pi} \tag{2.7}$$

or 1 nanohenry per cm. height of cavity.

Equations (2.6) and (2.7) can be obtained from most text books in electromagnetic theory with the understanding that $I_w = 2\pi a H_{\phi}$ at the wall.

$$\frac{\omega_0 L_0}{R_w} = \text{unloaded Q of cavity}$$
 (2.8)

How R₀ is related to the load will be dealt with in subsection 2.6.

2.3 EFFICIENCY.

The efficiency of the ARFCA depends on the efficiency of the individual SSD device and that of the combining structure. The overall efficiency is the product of the two. The combining efficiency can be obtained from the equivalent circuit of Figure 2-3. It is clear the combining efficiency R_{comb} is given by

$$\eta_{\text{comb}} = \frac{R_0}{R_0 + R_w} \tag{2.9}$$

Where wall loss R_w as given by (2.6) is at a fraction of R_s . At 1 GHz R_s is 8.25 m Ω for copper and 10.31 m Ω for aluminum. It can increase by a factor of 3 at X-band and decrease by a factor of 3 at VHF. Thus R_w is in the range of few milliohms. The value of R_0 is such that it would match with the number of transistors in parallel. Consider 20 devices are used and each is to be matched with 4Ω , R_0 is then 4/20 = 200 m Ω . The combining efficiency is then in the high 90% range, and can often be larger than 99%. At this level often other factors in the details of the physical fabrication will influence the actual performance.

2.4 BANDWIDTH.

The equivalent circuit used in Section 2.2 for calculating efficiency can also be used for determining bandwidth. The instantaneous bandwidth of the ARFCA is governed by its loaded Q factor with both source and load impedances taken into consideration:

$$Q = \frac{\omega_0 L_0}{R_0 + R_s + R_w} \tag{2.10}$$

Where R_s is the real part of the source impedance. In a matched system

$$R_s = R_o + R_w \cong R_0$$
, or

$$Q \cong \frac{\omega_0 L_0}{2R_0} \tag{2.11}$$

and

$$R_0 = \frac{R_t}{N}$$
 where R_t is the specified transistor load resistance.

Thus the 3dB bandwidth

$$\Delta f_3 = \frac{f_0}{Q}:$$

$$\Delta f_3 = \frac{2R_0}{2\pi L_0}$$

$$\Delta f_3 = \frac{2R_0}{2\pi L_0} \tag{2.12}$$

However when nonlinear SSD devices are involved such as Class C transistors, the concept of conjugate matching is usually not appropriate for loading consideration.

The value of the load impedance as specified in the device data book of the manufacturer usually represents an optimum of several criteria such as efficiency gain and bandwidth etc. The internal "resistance" of the device, representing some power absorbing mechanism within the device package, should be less than the real part of the specified Z_l . The actual bandwidth therefore should be a bit less than that given by (2.13) but more than $R_0/2\pi L_0$.

Hence in a typical 20 device ARFCA, at $R_0 \approx 200 \text{ m}\Omega$

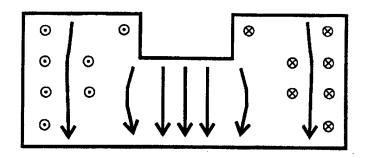
$$\Delta f_3 \le 400 \times 10^3 / 2 \pi \times 10^{-9} h \cong 63/h$$
 MHz where h is the height of the cavity in cm. (2.13)

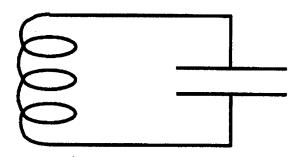
It is to be noted that, unlike a cavity based tube, there is no constraint on cavity height other than practical mechanical factors related to construction. Thus the bandwidth can be increased arbitrarily in principle to the limit by the BW of the device. Also there is the trade off between the number of the devices used or the value of the device impedance and the system bandwidth. In the example given earlier, $\Delta f_3 \leq 126/h$ MHz if 10 SSDs are used instead of 20.

2.5 TUNING.

The cylindrical cavity used for ARFCA can be tuned by a slug tuner as shown in Figure 2-4. The resonant frequency is lowered by a tuning slug in the configuration as shown. As the slug penetrates into the cavity, the EM field distribution will no longer be given by that of (2.1). A small E_r will begin to show resulting from the fringing along the edge of the slug, while magnetic field remains only with H_ϕ component. A z-dependence on both EM components will result. However the resonant frequency of this structure together with the filed distributions can be obtained accurately by the computer code SUPERFISH. The code also gives the energy stored and the power loss for a copper cavity wall at room temperature corresponding to a preset field amplitude. From this information values of L_0 , R_w , and C_0 in the equivalent circuit can all be determined: L_0 from the energy stored, R_0 from the power loss corrected by conductivity ratio of the material used for the cavity with that of copper, and C_0 from the L_0 and resonant frequency with the tuning slug in place.

TUNING:





SUPER FISH CODE:

$$\frac{1}{2}LI_{w}^{2} = U$$

$$\omega_{o} = \frac{1}{\sqrt{LC}}$$

$$I_{w} = 2\pi H_{\phi}$$

Figure 2-4. Slug tuner and resonant frequency.

 H_ϕ along the wall is expected to vary along the height of the cavity. Thus the $I_w = 2\pi a \ H_\phi$ in various equations should correspond to H_ϕ at the gap across which the SSDs are mounted. It can be shown that a large range of tuning can be accomplished. This fact can also be utilized to reduce the cavity size to a desirable size for lower frequency operation.

Intuitively, the tuning by the slug can be understood by using the sketches of the field lines of Figure 2-4. The electric field lines indicate the structure in the center portion of the cavity is capacitive formed approximately by the end face of the slug and the bottom of the cavity. The remaining portion of the cavity with the magnetic field lines as sketched represents approximately a three quarter turn inductor wrapped around and connected in parallel with the capacitor. As the slug penetrates deeper, the capacitance is increased. Simultaneously addition magnetic field lines begin to appear around the tuner side surface resulting in increasing inductance. The increase of both inductance and capacitance was born out by the SUPERFISH code calculations. As the tuner penetrates deep into the cavity such that its end face is separated from the bottom by a very narrow gap, the capacitance is then essential that of a parallel plate capacitor and the inductance be that of a short circuited coaxial line formed by the cavity wall and the tuner. By this approach a resonant cavity at 100 MHz, the diameter can be reduced from over two meters to about 20 cm with all other dimensions of the structure remaining completely reasonable.

2.6 COUPLING TO CAVITY VIA COAXIAL CABLE.

Coupling between the EM field in a resonant cavity and an external coaxial cable is well understood and has been considered textbook material⁶. However for ARFCA, the cavity also serves as a matching transformer. The main interest here is how to design a coupling loop or probe such that a coaxial transmission line of characteristic impedance of Z_o (say 50Ω) connected to a matched load, will manifest itself as the R_o at the gap. Thus between the gap and the coaxial connector a proper transformer will result.

Assuming that the system is at resonance and all reactance tuned out, and that the cavity losses are negligible, the conservation of power requires that

$$\frac{1}{2}|I_w|^2 R_0 = \frac{1}{2}|V_0|^2 / Z_0 \tag{2.14}$$

where V_0 = output voltage at the coaxial line.

$$I_{w} = 2\pi a H_{\varphi} |_{wall}$$

and

$$V_0 = j\omega\mu \iint_{loop} \vec{H} \cdot \vec{ds}$$
 for loop coupled

⁶ R.S. Harrington, "Time-Harmonic Electromagnetic Fields," Ch. 8, McGraw Hill, New York; 1961

$$V_0 = \int_{probe} \vec{E} \cdot \vec{dl}$$
 for probe coupled

From (2.15), one has

$$R_0 = \frac{\left|\frac{V_0}{I_w}\right|^2}{Z_0} \tag{2.15}$$

Since both V_o and I_w are proportional to the field amplitude, the ratio $|V_o/I_w|$ is a constant depending on the geometry of the cavity and that of the loop or the probe. For the cavity with a tuner slug, this ratio can be found through the SUPER FISH calculation. As an illustration we consider the case for a plain cylindrical cavity without the slug and the loop is located at the wall. Using Equation (1) we have:

$$|I_{w}| = 2\pi a \sqrt{\frac{\varepsilon}{\mu}} |E_{0}| J_{1}(2.405)$$

$$|V_{0}| = \omega_{0} \mu \sqrt{\frac{\varepsilon}{\mu}} |E_{0}| \iint_{\Delta A} J_{1}(kr) \vec{a}_{\phi} \cdot \vec{n} \ ds$$
(2.16)

where ΔA is the area covered by the loop and \vec{n} is its unit normal vector. If ΔA is small:

$$\begin{aligned} |V_0| &\cong \omega_0 \mu \sqrt{\frac{\varepsilon}{\mu}} |E_0| J_1(2.405) \Delta A \cos \alpha \\ \text{where } \cos \alpha &= \vec{a}_{\varphi} \cdot \vec{n}. \text{ Thus} \\ \left| \frac{V_0}{I_0} \right| &\cong \frac{\omega_0 \mu \Delta A \cos \alpha}{2\pi a} = \frac{2.405}{2} \left(\frac{\Delta A}{\pi a^2} \right) \cos \alpha \sqrt{\frac{\mu}{\varepsilon}} \\ \left| \frac{V_0}{I_w} \right| &\cong 453 \left(\frac{\Delta A}{\pi a^2} \right) \cos \alpha \text{ ohms} \end{aligned}$$
 (2.17)

It is seen therefore, by adjusting any number of factors, a coaxial line with a matched load can transformed into a large range of small values of R_0 .

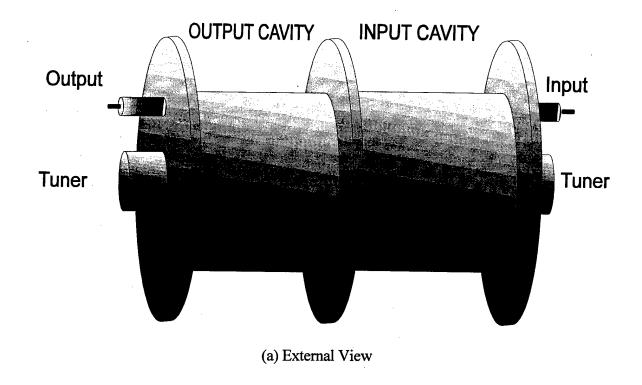
Not included in the above discussions is the effect of the self reactance of the loop or the probe. In order to achieve effective coupling, it is more desirable to have its effect tuned out independently. For example the self inductance of a loop is effectively in series with the impedance represented by the cavity mode. Therefore it would be much easier to use a series capacitance of appropriate value to tune out the self inductance. Much of these issues belong to the art of good engineering design and can only be dealt with as such.

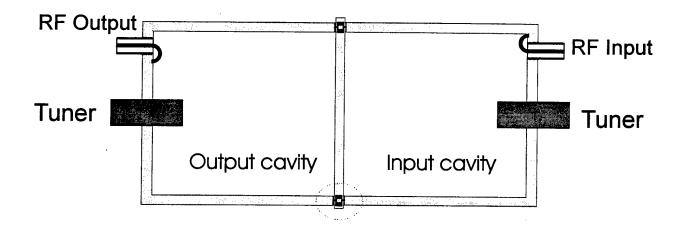
SECTION 3 A PRACTICAL DESIGN

In Section 2, we have given the basic principles for ARFCA operation. However in a practical amplifier the input mechanism is equally important. The ARFCA cavity approach can also be used for input, or as a "distributor."

Such a design is shown in a series of drawings Figures 3-1 - 3-4. Figure 3-1 (a) is the external view of a typical ARFCA showing essential components. It consists of two cavities separated by a center plate. Each is fitted with a coaxial connector and a tuner slug, for input and output power connections and for tuning. Transistors are mounted within the center plate with their input/output leads connected across a gap to the respective cavity wall as shown in the sectional view of Figure 3-1 (b). Figure 3-2 (a) shows a sectional view of the transistor mounted around in the center plate. Also shown are the tuner and the coupling coax connector. Figure 3-2 (b) is an enlarged detailed view of a transistor mounted within the center plate. The common electrode (base or emitter) which usually is the flange is physically in contact with the center plate. Cooling channels may be implemented within the center plate.

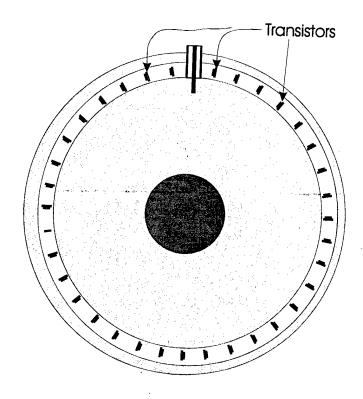
Figure 3-3 is a cut away view of practical ARFCA design consisting of six transistors. The drawing shows various components discussed earlier. It also consists of two items not yet mentioned. First is a quarter wave choke in the form of a slot cut into the cavity wall (item 5). A plastic (Teflon) insert (item 6) is used to shorten the physical length of the choke. The choke prevents the RF power from leaking out of the cavity and provides isolation for the dc bias source. A similar arrangement is implemented in the input cavity (obscured from view). The second item is how the transistors are mounted. They are positioned to be inserted into the receptacle openings (item 8) on the center plate. The transistor holder arrangement as depicted here is not the most desirable approach for many reasons. However it demonstrates the idea most clearly. Many other arrangements are possible including some with holders to be inserted from the side of the cavity effecting easy installation and removal. Figure 3-4 is another perspective of the same drawing.



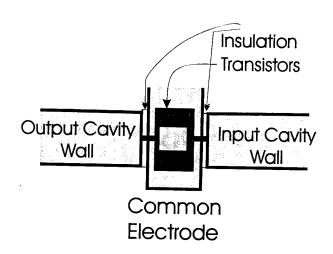


(b) Sectional view

Figure 3-1. ARFCA cavity external view (top) and sectional view (Bottom).



(a) Side view



(b) Transistor mounting

Figure 3-2. ARFCA cavity side view (top) and transistor mounting (bottom).

LEGEND

- 1. Tuner
- 2. Coaxial input/output
- 3. Coupling loop
- 4. Cavity end wall
- 5. Cavity side wall with slot cut into wall to accept six transistors. 5 + 6 is choke. Cooling fins optional.
- 6. Plastic insert
- 7. Center plate
- 8. Opening on center plate
- 9. Trnasistor holder, to be fitted into 8
- 10. Transistor
- 11. Teflon ring

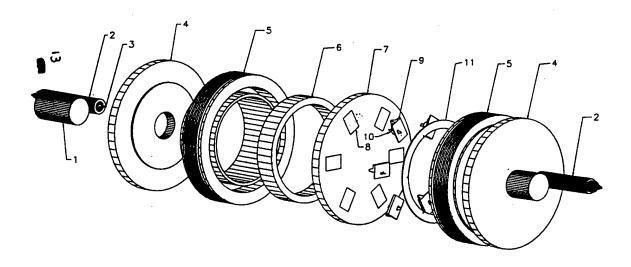


Figure 3-3. ARFCA components.

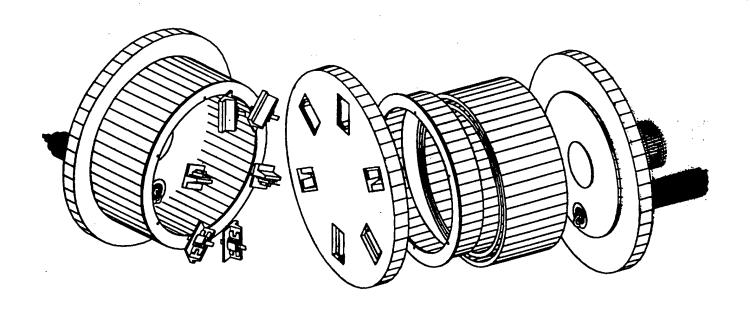


Figure 3-4. ARFCA assembly.

SECTION 4 PROTOTYPE ARFCA - EXPERIMENTAL RESULTS

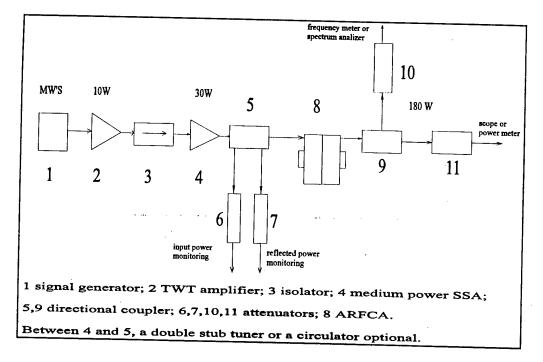
This section describes the development effort of a prototype ARFCA for proof of principle, and presents the experimental results. The development of a new RF solid state amplifier effort is generally known to be a trying process. Much trial and error is expected; and in the various process many experimental SSDs can self-destruct due to various instabilities⁷. Without past experience as a guide in the effort of a totally new RF amplifier technology, the process can be even more torturous than usual. It requires the combined knowledge and subtlety of solid state electronics circuit technology and electromagnetic theory/microwave engineering. For these reasons we chose at the beginning of the program, a physically small and relatively low power model as our prototype for proof of principle. This choice is driven primarily by economics and time limitations of the program. It can be argued that a larger cavity with larger number of devices may actually offer some advantages. Operation frequently is better when more transistors are used in parallel to drive the cavity. The proper load impedance seen at the gap is of the order of 1/N of the individual device output impedance where N is the number of devices used. Each device then approaches a current generator for large N and can then tolerate more device parameter variations.

In spite of that, we chose for the first model the operating frequency of 1.8 GHz with a cavity dimensions of 12 cm ID by height of 7 cm. At a frequency of 900 MHz, the dimension of the cavity would be twice as large. An outside independent machine shop must be engaged to fabricate the cavities. The cost of each model becomes much higher and the waiting time between models becomes much longer. The ad hoc changes usually very much needed will not likely be possible. We decided to use only six transistors for this model. We believe in the first attempt of this effort, it would be prudent to limit the scope of loss of transistors due to instabilities or other accidental events.

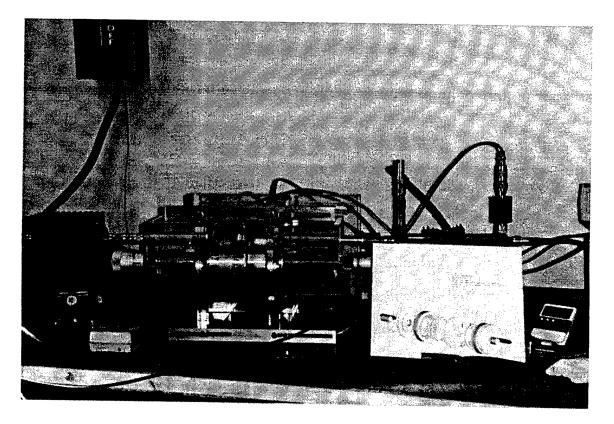
The preliminary success of a working model was achieved in Spring of 1995 with six class C common base SGS-Thomson AM81719-30 transistors at 1.8 GHz with a nominal output power of 30 W each. Over 150 watts of output was observed with a system overall gain of better than 7 dB. However, these transistors were soon accidentally destroyed during experiments. Supply was back logged over six months. The effort to find equivalent devices from other manufactures was unsuccessful. The demand of 1.8 GHz 30W devices at the time was particularly high. We finally decided to use the Motorola MRF16030 device which was designed originally for 1.6 -1.64 GHz but upgraded to 1.5 - 1.7 GHz.

The cavity was retuned to the lower frequency from the 1.8 GHz. Much effort was devoted to obtain the designs of the coupling loops. Most of the effort was spent in repeated cut and try until satisfactory performance was obtained.

⁷ N. Dye and Helge Granberg, "Radio Frequency Transistors, Principles and Applications," Motorola Series in Solid State Electronics, Ch. 7 Butterworth-Heinemann, Boston; 1993



(a) Schematic



(b) Photo

Figure 4-1. Experimental setup in schematic (top) and photo (bottom).

The experimental set up is as shown schematically together with a photograph of the model and the equipment in Figure 4-1. A low power signal generator, either a sweep frequency oscillator or a single frequency generator operated CW, pulsed or square wave, is first amplified by a wide band traveling wave tube amplifier to about 10 watts. It is further amplified by a home made SSD amplifier using the Thomson AM81719-30 device capable of 30W or higher, to drive the ARFCA prototype. The following summarizes the experimental results.

Motorola MRF 16030:8

Frequency: 1.5 -1.7 GHz Output Power: 30W nominal

Power Gain: 7.5 dB min., 7.7 dB typ Collector Efficiency: 40% min. 45% typ

Table 4-1 summarizes the earlier experiment with the cavity tuned for 1.68 GHz operation except the last entry with the highest power which is at 1.64 GHz. The last point of the 1.68 GHz data group was obtained with the highest input power obtainable from the homemade medium power driver amplifier. The driver was later modified with the aid of a double stub tuner and its output power was increase to near 40W at 1.64 GHz. The return loss was also increased. The input and output power data were averaged over six transistors and were plotted in the Motorola data book graphs for P_{out} vs. P_{in} as shown in Figure 4-2. It is seen that these points fall above the curves for the 1.6 GHz and 1.64 GHz. One may surmise that the cavity is less lossy than the microstrip line based circuitry used for device testing by the manufacturer.

Table 4-2 and graphs with data points shown in Figure 4-3 summarizes a second set of experiments carried out after the original setup and the ARFCA model were first disassembled, and reassembled sometime later. The cavity was retuned for 1.7 GHz and the results are essentially the same as those of the first set.

These results thus have conclusively proved the ARFCA principle. It should also be noted that the prototype was assembled completely with hand tools without soldering. The only discrete passive electronics components needed were the few capacitors used for decoupling the collector power supply.

It is also of interest to note that the measured 1 dB bandwidth is approximately 6 MHz. Using the cavity dimensions and the published device impedance, the calculated 3 dB bandwidth is 11.36 MHz, or the 1 dB bandwidth of 5.68 MHz.

⁸ Motorola Inc. "RF Device Data," DL110/D Rev 7 pp. 2-837 to 2-840; 1996

ARFCA PRE-PROTOTYPE "Proof of Principle" 12.5 cm D X 7 cm H

6 transistors 1.8 GHz, 180 W cw

Transistor :

Motorola MRF 16030

Frequency

1.60 - 1.64 GHz

Nominal Pout

30 W

Gain:

7.5 dB min.

7.7 dB typ

 η_c

40% min. 45% typ

Experimental

frequency

1.68 GHz

		quency	•	1.00 01	. 1 <i>Z</i> .		
P _{in} , W	$P_{r,}$	P _{out}	V _{cc} ,	I _c , A	P _{dc} ,W	η,	G _p , dB
(1)	W	(1)	V	(2)	(2)	%	(3)
19.5 (3.25)	2.4	118.7 (19.8)	25	5.6	140	42.4	7.8 (8.4)
20.4 (3.40)	2.6	124.8 (20.8)	25	5.8	145	43.0	7.9 (8.5)
20.0 (3.33)	2.1	134.9 (22.5)	27	6.0	162	41.6	8.3 (8.8)
21.6 (3.60)	2.3	140.3 (23.4)	27	6.2	167	42.0	8.1 (8.6)
23.7 (3.95)	2.8	151.1 (25.1)	27	6.6	178	42.4	8.0 (8.6)
23.7 (3.95)	2.7	156.5 (26.0)	28	6.8	190	41.2	8.2 (8.7)
*39.0 (6.50)	9.8	188.9 (31.5)	28	7.2	202	46.8	6.9 (8.1)

- (1) Numerical values in parenthesis are per transistor
- (2) Square wave modulation, 50% DF
- Numerical values in parenthesis represent G_p when P_r is subtracted from P_{in}
- * 1.64 GHz, Driver amplifier was modified to increase output power. Modification also increased mismatch.

MRF 16030

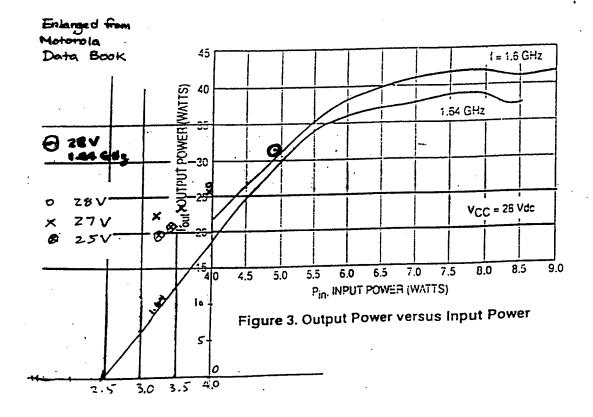


Figure 4-2. ARFCA Experimental results 1.68 GHz.

Table 4-2. ARFCA experimental results 1.8 GHz model - 6 transistors.

Single transistor

								emgle train	
Pout W	Pin W	Pref W	Pin(net) W	Gp dB	Gp* dB	DCP W	eff. %	Pi W	Po W
198.2	32.7	3.7	29.0	7.8	8.4	436.8	45.4	4.8	33.0
192.3	31.7	3.5	28.2	7.8	8.3	414.4	46.4	4.7	32.0
186.4	30.8	3.4	27.4	7.8	8.3	397.6	46.9	4.6	31.1
183.4	29.9	3.3	26.6	7.9	8.4	386.4	47.5	4.4	30.6
177.5	28.9	3.2	25.7	7.9	8.4	380.8	46.6	4.3	29.6
168.6	28.0	3.1	24.9	7.8	8.3	358.4	47.0	4.2	28.1
165.7	27.1	3.0	24.1	7.9	8.4	347.2	47.7	4.0	27.6

^{*} Reflected power subtracted from input power

P_{in(net)}=P_{in} - Pref

Pout, Pin & Pref measured at input/output connectors

 $P_i = P_{in(net)}/6$

P_o=P_{out}/6

Frequency=1.7055GHz Instant 1db Bandwidth~6MHz 6 Motorola MRF 16030 transistors

Graph scanned from Motorola RF device data book Q1/96 DL110 Rev7

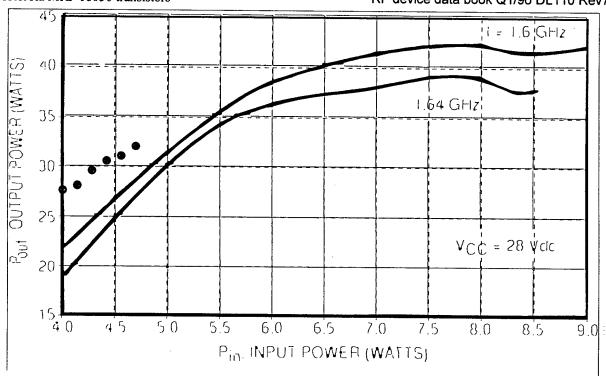


Figure 4-3. ARFCA Experimental results 1.7055 GHz.

SECTION 5 HIGH POWER PROTOTYPE

A high power ARFCA model development effort began nearly a year ago. The model is designed for the industrial frequency of 915 MHz at 1.0 - 1.2 kW power output. The model consists of 20 Motorola MRF 898 devices which yields a nominal 60W output each with saturation power at about 75 W. The following is a summery of its electrical characteristics:

Transistor : Motorola MRF 898

Frequency : 915 MHz Nominal Pout : 60 W

Gain: : 7 dB min. 7.9 dB typ

 η_c : 60%

Operation : Class C common base

 V_{cc} : 24 V Z_{in} @915MHz : 7.2-j1.3 Ω Z_L^* @915MHz : 4.5+j2.0 Ω

Cavity dimensions is 30 cm diameter by 17 cm height. The design has the following features and may lead to the first production model.

Design features:

- Transistors first mounted in holders which are inserted into or removed from the cavity structure with ease.
- Assembling by hand tools. No soldering.
- Minimal post-assembly tuning. Low level labor skill and facility.
- Water-cooled, $T_j < 100^{\circ} C$
- P_{out}: 1.2 kW @ 60% efficiency
- $G_p \approx 8 \text{ dB}$

At present the experimental results have indicated that the basic ARFCA principle holds equally well for a 20 device model. Over 250 W of output power has been reached. Attempt to drive it further would lead to instability and often device destruction. With the aid of a spectrum analyzer (on loan from Polytechnic University) we identified it to be the so called fo/2 varactor oscillation. This instability is well known in general as the parametric decay instability in the degenerate case that the pump frequency is twice the oscillating frequency. We are currently working with a Motorola engineer informally, on means to suppress this oscillation. We expect the resolution of this issue soon. In the mean time we are exploring alternative device choices. The Ericsson PTB 20167 which has the same characteristics as the MRF898. It is regarded as the "more stable" by a few RF power engineers in the community.

SECTION 6 COMMERICIALIZATION

Aria Microwave Systems (AMS) has made continuous efforts to commercialize the ARFCA technology throughout the contract period. The technology has been presented to many parties: individuals, other government agencies and small and large corporations. The results have so far not developed into concrete commitments for a number of reasons.

6.1 HISTORY OF COMMERCIALIZATION.

The early history of commercialization efforts began at the inception of the Phase II contract. We worked with Technology Management & Funding L.P., Inc. of Princeton New Jersey (TMF) until Spring of 1995 to seek commercialization funding. Early in 1994 we met with several companies to present the ARFCA concept. The purpose at this time was to seek joint development funding for niche markets. Some larger companies were contacted as well, but found that the technology either was not suitable or they were reluctant to approach an unknown.

Toward the last half of 1994, Philips Semiconductors became interested in the ARFCA technology for HDTV (high definition television) development. After months of discussions and meetings, Philips decided that they could not invest in the ARFCA technology. The implementation of terrestrial broadcasting HDTV was stalled for several reasons. Its future is still cloudy.

In the mean time, a small ARFCA prototype with six transistors was completed and the ARFCA concept was proven. We also became aware of a wide spectrum of possible applications for ARFCA at different power levels and frequencies. One of these was at the frequency of 915 MHz which is used by several applications including industrial heating.

Companies such as DuPont, 3M, Amana/Raytheon, IBM and Cober Electronics are extremely interested in purchasing ARFCAs at the 915 MHz frequency range. It was then decided to develop the next prototype at this frequency and to consider developing a small manufacturing facility once the prototype was completed.

During the past two years, AMS has worked with a consulting team, International Power Strategies, that has provided marketing information and contacts, analysis of the different markets and other consulting. They are also helping AMS develop a business plan to carry forward our commercialization efforts. The plan is incomplete at this writing, but sections have been included in this report. Appendix XX is a Marketing Strategy program that they developed.

6.2 APPLICATIONS.

The following are applications under extensive evaluation:

- Industrial heating Because of the availability of the low cost magnetrons, rf/microwave heating has become principal heating sources in many industrial processes. The applications include: heat treatment of metals, shrinking of tubing, coating, melting, hazardous waste disposal, crystal growing, carbon vapor deposition, levitation and external deposition and various plasma processing
- Radar In radar systems such as air traffic control, weather radar and some military systems, nearly continuous operations are required making the long life and high reliability of SSDs highly desirable. Currently most systems use tube technology for generating the rf power required. Other advantages in SSDs/ARFCA include its small size, light weight, low voltage and low cost.
- Electrode-less-bulb Plasma lighting In recent years, new electrode-less light sources have been developed to overcome some of the problems inherent in conventional lamps. The Philips QL, GE Genura and Fusion Lighting Sulphur bulbs all use induction technology and microwave excitation to operate. Manufacturers use magnetrons in high power large scale applications.
- FM broadcasting and digital audio broadcasting (88 108 MHz, VHF) Kilowatt level power is required for terrestrial broadcasting and tubes are currently the only sources which presently serve this industry. The world wide growth of FM broadcasting, especially in the third world areas and their need for a SSD RF power source can mean an important market for ARFCA.

6.3 STRATEGIC MARKETING PLAN.

AMS will utilize four distinct approaches for the commercialization of ARFCA technologies depending on the characteristics and dynamics of each market area.

6.3.1. Internal Funded Product Development and Manufacture.

- Work with selected customers for the ARFCA product to determine system requirements such as thermal management, control, interfaces, and packaging;
- Provide prototypes for customer evaluation and final requirements;
- Use local suppliers to manufacture various hardware components of the ARFCA units, use commercially available transistors and other components;
- Own final assembly manufacturing facilities to Assemble and Test the ARFCA product;
- Use selected Manufacturers Reps for direct sales and service to target customers who will incorporate the units into their internally designed process facilities;

• Price the product based on the value of the advantages provided by the ARFCA technology (Solid State reliability, low voltage power supplies, no vacuum, graceful degradation, etc.).

This approach will be used in selected market niches where the benefits provided by the ARFCA technology are recognized by the customer, the market volume is relatively modest and the number of initial customers is limited. Target markets include the high end of the Industrial Processing industry with applications in the chemical, pharmaceutical and semiconductor segments. Initial target customers include Dow Chemical, DuPont, 3M, and IBM. These market segments typically operate their processes at 915 MHz and require units with 500 watts to several kilowatts.

- 6.3.2. Strategic Partnering With Well Positioned Component Supplier To OEMs.
 - The strategic partner(s) will generally already be providing tube based RF amplifiers to the OEM markets;
 - AMS would bring in the technology to expand their existing product lines with high power solid state RF amplifiers;
 - The partner would fund development of ARFCA products that meet the needs of selected segments of their current customer base;
 - AMS would develop the products to prototype versions and support the final product design and manufacture by the partner;
 - AMS would provide input for cost reduction, new product development and support;
 - The partner would be responsible for product manufacture, product pricing, sales and support;
 - AMS would receive compensation based on licensing of the technology and royalties from product sales.

This approach will be used in selected market niches where the benefits provided by the ARFCA technology are recognized by the end customer, the market volume is modest and the number of initial customers is limited. Target strategic partners would already have good position in serving the markets (with tube-based products) and are willing to invest in ARFCA technology to strengthen their position as a supplier to the market by expanding their product lines by acquiring rights to manufacture and introduce solid state products to their customer base.

- 6.3.3 Strategic Partnering With OEMs That Would Benefit From Having Exclusive Use of ARFCA Technology In Their Products.
 - The strategic partner(s) will generally already be providing tube based RF amplifiers to the OEM markets;
 - AMS would bring in the technology to expand their existing product lines with a high power solid state RF amplifiers;
 - The partner would fund development of ARFCA products that meet the needs of selected segments of their current customer base;

- AMS would develop the products to prototype versions and support the final product design and manufacture by the partner;
- AMS would provide input for cost reduction, new product development and support;
- The partner would be responsible for product manufacture, product pricing, sales and support;
- AMS would receive compensation based on licensing of the technology and royalties from product sales

This approach will be used in selected market niches where the benefits provided by the ARFCA technology are recognized by the partner and will result in product differentiation and potential of expanded market applications. Target strategic partners would already have good position in serving their markets (with tube-based products) or are introducing a new line of products that will have increased market acceptance because of the benefits that ARFCA technology would bring to the product realization. The partner would be willing to invest in ARFCA technology to strengthen their position as a supplier to the marketplace. Potential partners include suppliers of microwave powered light sources and suppliers of radar systems.

- 6.3.4 Seek New Government Programs That Are Advertised Through A Request For Quote (RFQ) Or Request For Proposal (RFP) Process Which Provide Opportunity For AMS To Apply The ARFCA Technology And Benefit The Application.
 - If the project has limited scope and can be generally satisfied with an ARFCA product, AMS may directly apply for the project;
 - If the project has broader scope but can significantly benefit from inclusion of the ARFCA technology, AMS may identify a major company already interested in becoming the Prime Contractor and AMS would be a sub-contractor to the Prime and provide the ARFCA technology.

6.4 ENABLING TECHNOLOGIES.

The characteristics of ARFCA are those of the particular SSDs used. Thus each particular application requires a certain kind of performance which is specific to the application. In many cases satisfactory level of performance can be achieved in the off-the-shelf devices. On the other hand, devices with their electric characteristics are often appropriate, but in unsuitable packaging. Sometimes devices which were once available are withdrawn from the market by the manufacturer. In special cases, new devices need to be developed. These critical issues point to the need of collaboration with device manufacturers It would be of great advantage if synergistic business relations could be structured with SSD manufacturers which emphasize technology R & D cooperation in addition to other regular business issues.

In general, the RF power transistor industry is presently still evolving. Except the two giant companies, Motorola and Philips, the other manufacturers are all relatively small whether they are independent operations or affiliates with major corporations. The management of these operations have shown interest and eagerness in cooperating once they became aware of the potential of ARFCA. We are in the process of establishing such a relationship with one of these companies for a class of rf devices which will be of critical importance to the industrial applications.

6.5 SUMMARY.

Although at the conclusion of this contract Aria Microwave Systems will be without external funding, we continue operating to complete the 915 MHz prototype and upon completion of the business plan will continue to pursue commercialization.

APPENDIX A LIST OF ABBREVIATIONS, ACRONYMS AND SYMBOLS

Active radio frequency cavity Active radio frequency cavity amplifier Alternating current Aria Microwave Systems Capacitance Centimeters Circuit quality	ARFC ARFCA AC AMS C cm	Radio frequency Representative Request for proposal Request for quotation Resistance Resistance inductance capacitance circuit Solid state device	RF or rf reps. RFP RFQ R RLC Circuit SSD
Continuous wave	CW	Solid state power amplifier	SSPA
Cross section loop area	ΔA	Transient mode number	TM xxx
Current	I	Typical	typ.
Decibel	dB	Voltage	V
Direct current	DC	Watts	W
Efficiency	η		• •
Efficiency	eff.		
Electric field	E		
Exterior diameter	OD		
Frequency modulation	FM or fm		
Gigahertz	GHz		
Impedance	Z		
Inductance	L		
Interior diameter	ID		
Kilowatt	kW		
Loop angle	α		
Magnetic field	H		
Megahertz	MHz		
Milliohms	m Ω		
Millimeters	mm		
Not invented here	NIH		
Ohms	Ω		
Original equipment manufacturing	OEM		
Permeability constant	3		
Permittivity constant	μ		
Power goin	P C=		
Power gain	Gp		

APPENDIX B

PHASE I RESULTS INITIAL APPLICATIONS FOR ARFCA

James M. Fletcher Joseph J. Horzepa Nicholas Osifchin

AMS Phase 1 Results

INITIAL APPLICATIONS FOR ARFCA TECHNOLOGY

The Marketing Agreement between Aria Microwave Systems (AMS) and International Power Strategies calls for a report covering results of Phase 1 of the basic proposal which states:

Define and prioritize the market niches that appear to provide the highest potential for application of Aria Microwave Systems products;

This effort will develop an exhaustive listing of all the potential applications that can be identified in one or more sessions between representatives of AMS's management team and IPS. This step will result in a prioritized list of the most promising market niches based on criteria developed during the working sessions.

The initial meeting with the ARFCA management team was held on April 19, 1995 and the notes from that meeting are summarized in a memo "ARIA KICK-OFF MEETING" which was distributed to all attendees. The Phase 1 report reflects all of the meetings and discussions between representatives of AMS's management team and IPS plus the face-to-face meetings, telephone conferences and Faxes exchanged with Neil Wilson on military and government applications. In addition, a number of face-to-face and telephone conferences were held with key researchers at Bell Labs and MA-CON. A literature search was also done of pertinent trade and technical journals and manufacturers catalogs.

The following items were identified as the criteria that should be used in evaluating the relative potential of applications for ARFCA Technology:

Technical requirements consistent with ARFCA capability

Size of Market;

Relative Growth Rate of Market:

Willingness of Market to consider new technologies;

Tolerance to technology risk;

Relative value of power amplifier to total system costs.

The Phase 1 report is presented in chart form for ease in preparation and to enhance its usefulness in discussions as additional information becomes available. The contents of each chart is as follows:

Chart 1	POTENTIAL APPLICATIONS CONSIDERED FOR ARFCA TECHNOLOGY
Chart 2	MARKET NICHES THAT PROVIDE THE MOST PROMISING POTENTIAL FOR APPLICATION OF ARFCA TECHNOLOGY
Chart 3	OVERVIEW AND COMMENTS ON POTENTIAL APPLICATIONS
Chart 4	GENERAL RF AMPLIFIER ATTRIBUTES VS ARFCA
Chart 5	COMPARISON OF ARFCA TECHNOLOGY VERSUS EXISTING

IPS is currently working on the remaining steps listed in the Marketing Agreement to identify the potential End Users in each market niche listed in Tiers 1 and 2 and the specific OEMs that are currently supplying products to those End Users. At the same time, the general requirements that an ARFCA device must satisfy for each potential application will be determined for discussion and evaluation with the AMS management team.

CHART 1

POTENTIAL APPLICATIONS CONSIDERED FOR ARFCA TECHNOLOGY

Television Digital TV HDTV

Telecom

PCS

Cellular (AMPS, GSM)

Analog

Digital

Satellite

LANs

Military Communications

Satellite Up Link

Singars (single channel)

MSE (multiple subscriber equipment)

Electronic Warfare

Decoys

Spot Jammers

Radar

Airborne weather

ILS (instrument landing systems)

ATC (air traffic control)

Marine

IFF (identification friend or foe)

Fire Finder

Cobra

Active Aperture Radars

Aircraft beacons

Collision Avoidance

Medical

Medical Diathermy

Other Portable Medical Applications

CHART 2

MARKET NICHES THAT PROVIDE THE MOST PROMISING POTENTIAL FOR APPLICATION OF ARFCA

TIER 1 APPLICATIONS:

COMMENTS

Digital TV

The early success of DBS has stimulated heightened interest in this technology now competing with HDTV for introduction. Would require replacement of existing trans-

mission facilities - similar to HDTV

HDTV

Losing some momentum; may be slower roll out and implementation than expected last

year.

Cellular Telephone

Base Stations

Currently using SSA technology; OEMs have accepted the low efficiency resulting from combining up to 20 modules for 3 kW applications; very cost sensitive; low efficiency is a factor outside US. Opportunity is for new Cell Sites as well as upgrading existing sites for

Digital capability.

TIER 2 APPLICATIONS:

IFF - Identification Friend or Foe

Greatest potential is for ground based

transmitter sites.

Radar Air Traffic Control

Potential is for new sites, replacement of tube

amplifiers in existing installations as they be

come upgraded.

Other applications may be uncovered and qualify for high tier potential during the evaluation of the ones listed above or from continuing discussions with people in the military and commercial industries.

CHART 3

OVERVIEW AND COMMENTS ON POTENTIAL APPLICATIONS

APPLICATION	FREQUENCY	POWER LEVELS	BANDWIDTH	LINEARITY	COMMENTS
IFF - Identification Friend or Foe				. :	
- Intermediate Transponder	1030-1090 MHz	10's Watts Avg. 500 Watts Peak	60 MHz	•.	Uses Binary Coding. Prime US Suppliers include: Hazelfine and T-MEC
- Airborne Transponder	1030-1090 MHz	10 Watts Peak			Principle Supplier: Allied Signal (Bendix) in Towson MD
- Ground Based Transponder	1030-1090 MHz	5 kW Peak			Principle Supplier: Allied Signal (Bendix) in Towson MD
Wireless Telecommuni- cations					
- AMPS Cellular Base Stations	850-900 MHz	300 Watts Avg. 3 kW Peak	33 MHz	-60 dB in 30 kHz channel	Must replace SSA s, cost sensitivre application.
- PCS Base Stations	2 GHz	10,s Watts Avg. 1 kw Peak	75 MHz		Rapid growth expected over next 3 years.

CHART 3

OVERVIEW AND COMMENTS ON POTENTIAL APPLICATIONS (conf.)

APPLICATION	FREQUENCY	POWER LEVELS	BANDWIDTH	LINEARITY	COMMENTS
Frequency Hopper	900-928 MHz	1.0 Watt		. •	Flam-Russell, PA offers high power passive combiner for higher power
Radars	Fire Finder X Band C Band S Band	All fall in the kW power range	1GHz 500 MHz 300-400 Mhz		Upgrade of current systems now using high power tubes; no specific transmitter being defined at this time; only a requirements document

CHART 4

GENERAL RF AMPLIFIER ATTRIBUTES VS ARFCA

RF AMP	ARFCA
OUTPUT POWER	500 Watts to 20 kW
OPERATING FREQUENCY RANGE	400 MHz to 2.2 GHz
BAND WIDTH .	1% TO 2%
LINEARITY	
PHASE DISTORTION	
EFFICIENCY (PLUG TO OUTPUT)	~80%
FAILURE MODE	DEGRADES GRACEFULLY
RELIABILITY	SEMICONDUCTOR LIFE
POWER COMBINING	EFFICIENT, SIMPLE
POWER SUPPLY	ONLY LOW VOLTAGE REQUIRED
PHYSICAL CHARACTERISTICS: SIZE VACUUM SCALABILITY THERMAL RUGGEDNESS MANUFACTURE	COMPACT, NONE 1/f ² STATE OF ART ROBUST LOW COST

CHART 5

COMPARISON OF ARFCA TECHNOLOGY VERSUS EXISTING TECHNOLOGY PRODUCTS

		•										
	POWER	FREGUENCY	BAND	LINEARITY	PHASE DISTORTION	EFFICIENCY	THERMAL MGMT.	SIZE	RELIABILITY	cost	MANU. FACTURE	RF POWER COMBIN'G
ARFCA	2	2	2	-	_	2	_	_	-	_	-	-
KLYSTRODE	-	_	2	_	-	2		3	, 3 °	3	2	3
CC/TWT		-	_	_	-	2	-	3	. 3	င	2	င
SOUD STATE AMPLIFIER	3	2	-	-	e	e.	2	2	2	က	2	m

ARFCA technology provides all of the desirable attributes of Solid State Amplifier solutions (high reliability, manufacturability, low cost, small size) at significantly higher power levels with out the problems of the Solid State Amplifier technology. ARFCA technology provides all of the desirable attributes of tube technologies but at lower power levels, without need for vacuum, and without the need for multiple external components (i.e. power supply). Across the board, ARFCA technology appears to provide best efficiency, excellent linearity, and bandwidth comparable to Solid State Amplifier technologies.

COMPARISON OF ARFCA TECHNOLOGY VERSUS EXISTING TECHNOLOGY PRODUCTS

	POWER	FREQUENCY	BAND	LINEARITY	PHASE	EFFICIENCY	THERMAL MGMT.	SIZE	RELIABILITY	COST	MANU. FACTURE	RF POWER COMBIN'G
ARFCA	2	2	2	-		2	_	1	-	ı	1	_
KLYSTRODE	_	-	2	1	-	2	_	3	3	3	2	3
CC/TWT		-	_	-	-	2	-	3	. 3	3	2	3
SOUD STATE AMPLIFIER	3	2	-	-	3	ဗ	2	2	2	က	2	က

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CHART 5

APPENDIX C

AN ANALYSIS OF SOLID STATE TECHNOLOGY IN COMPARISON TO VACUUM TUBES

L. WAYNE CHEO

INTRODUCTION:

The purpose of this analysis is to provide insight in to current and future capabilities of microwave solid state power amplifiers (SSPA) and estimates into their future performances over the next ten years based upon the existing technology, and then explore the impact ARFCA technology will have on this existing technology and future Solid State Power Amplifier Technologies.

Currently solid state power amplifiers (SSPA) limitations are dependent on the performance of the transistors available and the efficiency and practical usefulness of the combining techniques. Because of these limitations it will be shown that current performance specifications based upon those technologies, have pretty much reached their limit and are not expected to increase dramatically in the near future. Furthermore, it will be shown that dramatic improvements in performance can be achieved through the application of ARFCA technology.

There will be four sections involved in this analysis, first an explanation of current transistor technology available, second an description of current combining technology, third, an analysis of current radar and communications applications now available, and finally a concluding analysis of the effects of ARFCA technology based upon the previous analysis.

I] THE TRANSISTORS.

The purpose of this section is to describe the current state of the art of in transistor technology and to examine the performance limitations of this current technology.

SILICON BIPOLAR TRANSISTORS:

Silicon Bipolar Transistors, used in both CW and pulsed applications, are mostly used in frequencies less than 3 GHz. The upper frequency limit is determined by the carrier mobility of silicon and the physical dimensions of the transistor. The Output power is limited by the breakdown voltage and heat considerations.

A Typical example of this transistor characteristics are at 2.8-2.9 GHz. to have 105 watts output power, with a pulse width of 50 micro seconds with a duty cycle of 10%, a gain of 6.5 dB and 35% efficiency.

GaAs FET's:

Today's standards for internally matched MESFET's have been set by the Japanese manufactures. On chip combining is achieved by matching at the input/output using chip capacitors, via holes and distributed elements. Typically IM-MESFET's achieve greater than 6 dB of gain with 25 % efficiency for most popular communication frequencies.

The power output is limited by the voltage applicable to the narrow gate, source, and drain elements. Because of these limits, it operates in both CW and pulsed modes with out any appreciable increase in power. Because of these physical limitations performance improvements in the future are not expected.

The power is also inversely proportional to the square of the frequency. For example in C/S bands, 2-6 GHz, power is in to 10 to 30 watt range typically at a cost of 300 to 900 dollars per unit. However in the Ka band, the power output is in the 2 watt range with cost upwards of 1500 dollars, and for Ku band, 12 - 14 GHz, the power range is in the 10 - 15 watt range with unit costs ranging from 1000 - 1500 dollars.

GaAs HEMT's (High Electron mobility transistor)

Though HEMT's feature high gain with increased efficiency over FET's of the same frequency specs, they are a new technology and difficult to make due to the good electron transport properties from the reduced impurity scattering.

HEMT's and PHMET's (pseudomorphic HMET) have allowed 5 watts of power output, with 12 dB of gain with 60 % efficiency at 4 GHz. Cost prohibitions will come down as the technology matures and it can be expected that large power consisting of internally combined HEMT's will be available.

GaAs HBT's (Heterojunction bipolar transistors)

HBT's show a lot of promise in the microwave frequencies because they can operate in class B or C modes at high gain and high power efficiency, with out exotic and expensive lithography. Typically, once can expect 0.5 watts and 11 dB gain with 60 % efficiency in class AB mode at around 10 GHz and 5 watts with 10 dB gain and 40 % efficiency in X band 8 - 12 GHz.

Phase array radar is the most probable application for HBT's in class B or C amplifiers, where efficiency and size are the principal requirements.

MMIC's (Monolithic Microwave Integrated Circuits)

MMIC's consist of a large number of transistor cells combined on a chip together with other circuit elements such as attenuators, power drives and switches.

Typically, MMIC's exhibit capabilities similar to those described previously for the discrete devices combined. For example MESFET's operating at 2 GHz, may run at 10 watts, in the 10 GHz range may output 6 watts and in the 50 GHz range may output 0.2 watts. Where as a HEMT operating in the 10 GHz range may output 10 watts and if operating in the 30 GHz range may output 0.5 watts.

Future outputs of MMIC power amplifiers are expected to increase by factors of to five because of combining techniques and are expected to dominate applications that require compact size and also mm wave operations.

SUMMARY:

The vast majority of applications that involve ARFCA technology consist of taking the existing transistor technology and combining them into a cavity wall and there by combining the available power to fulfill these high power applications. It is seen given conventional transistor packaging technology that ARFCA will be compatible with all transistors available current and future.

Higher frequencies, 3 GHz and up, can easily be achieved by using higher order modes of the ARFCA cavity, and therefore with an increased diameter, the cavity can accommodate many more transistors yielding much higher power outputs, while only using one stage to combine power.

II] COMBINING TECHNIQUES

There are four basic types of combining techniques outlined here. They are Wilkinson Combiners, Serial Combining, spatial field combining, and radial combining.

WILKINSON COMBINING

Often called 3 dB hybrid couplers the Wilkinson combiner is arranged in a pyramid structure of binary levels on a stripline structure. It most often uses 2 to 4 devices in combination. Larger numbers, 8 or 16, will suffer so much additional loss that the device is negated in usefulness due negation of gain or thermal considerations.

SERIAL COMBINING

Serial combining is taking output of the devices and serially combining it with output of a long transmission line. The values of the couplers are selected for equal power to and from each amplifier. Advantages of serial combining are element to element isolation, operation with a possible odd number of devices. Problems are the necessity of a long slim transmission line, and the phase problems associated with that, however for active aperture radar it is desirable.

SPATIAL FIELD COMBINING

Spatial field combining is a three dimensional scheme that transforms multiple inputs from a coaxial TEM mode through stepped impedance's of balanced spatial TEM modes, to a single coaxial output.

The combining efficiency is greater than 90 % and though bulky, can handle up to 30 watts in Ku band and 250 watts in S/C bands. It also can be used with mini TWT's

RADIAL COMBING

Inputs of a radial combiner are place in circular symmetry and combined in the center output port. These radial lines must provide the impedance transformations and are fabricated in a parallel plate or stripline structure.

Radial combiners can have as many as 15 - 20 inputs and provide modest isolation between the ports. Due to the geometry many problems with standard packaging and cooling exist.

SUMMARY:

The necessity of power combining comes from the limitations of the output power of the transistor. When large RF power is needed transistors must be combined, however efficiency problems occur in the final stages of combining due to the vast number's of transistor required to achieve high power.

In the final stage of amplification of high power systems, large numbers of transistors (on the order of 50 - 200) require combining in order to achieve the necessary levels of power, (of the order of 10 kilowatts or higher) efficiency becomes a very important issue. In ARFCA technology all or a large number of transistors are combined at one stage and the measure of efficiency is only located in the efficiency of the transistor and the effective loss in the cavity wall, instead of the layers of networks necessary in other devices.

III] RADAR APPLICATIONS

CORPORATE FEED RADAR APPLICATIONS

Solid state transmitters are candidates for S band and lower frequency radar systems where uninterrupted operation and graceful degradation as well as hot maintenance are requirements. Airport surveillance radar ILS (Instrument Landing Systems) and ATC (air traffic control) radars are among these.

Current requirement are 12 kW peak power at S band for the Marine Air Traffic Control systems. Four Si Bipolar transistor rated at 100 watts but used at 85 watts (thermal considerations) are used in high power amplifier modules with a total rating of 300 watts are then combined via a stripline network to five 3.5 kW's of output. Four of these are in turn combined in a magic T network to give the 12 kW of power required and achieves a 61 % efficiency past the transistor. It must also be mentioned that the approximate limit in power has been achieved.

ACTIVE APERTURE RADAR

Specifically the power amplifier capability at X band currently is about 10 W from the available devices combined on chip or in microstrip circuits. For example 10 W has been achieved in the 8-14 GHz range using MESFET MMIC's in a serial combiner/divider network. This system is well suited for the insertion behind each antenna element of a phase array system. The T/R module performance in X band airborne applications are 8 watts at 7.5 - 10 GHz with a duty cycle of 40 % and efficiency of 20%. Systems can include as many 1200 - 2000 modules in structures 36 inches across.

The primary issue with solid state arrays is cost, at 400 dollars a module and 2000 modules it is easy to see why. 48% of the cost of a module is taken up by the MMIC, 17 % by the housing and substrate, 12 % in assembly and 23% in testing.

Future T/S modules will have some increase in power, but the most important issue is the reduction of cost.

MISSILE SEEKING RADARS

These include smaller air to air and air to ground systems. For example the Phoenix missiles uses GaAs IMPATT diodes in a cavity to produce 100 watts of pulsed power in X band,

but will be replaced with an AMRAMM which uses a tube system with higher power and thus greater range.

COMMUNICATION APPLICATIONS:

The main communications application where solid state amplifiers will compete with TWT's is in satellite earth stations. The commercial unlink systems are at C and Ku bands with Ka band planned for future systems. In addition, SATCOM are at low X band and MILSTAR will be at EHF (44 GHz.).

Solid state amplifiers are used extensively in low power, low data rate systems where 10's of watts are sufficient outputs. These systems use IM-MESFET's and stripline combining because IM-FET's have modest gain, the number of devices combined practically is four to minimize the loss in the combining network. At 10 volt operation the reliability is 1,000,000 hours MTBE.

SUMMARY:

The majority of truly high power application that can directly be addressed by ARFCA technology exist in the high power radar fields where conventional technology has reached it's practical limits due the levels of combining have reached the point where no matter how many more transistors are added the added levels of combining no longer increases the output. It is in this area that ARFCA makes it's most significant impact.

Another area that ARFCA technology can be used in the emerging area of High Definition Television. The UHF frequency range, and high power requirements of broadcast stations make ARFCA a natural contender to fulfill these special requirements.

IV THE FUTURE

The future of SSPA capabilities can be seen as the capability will increase only a few dB. The main focus will be in lower cost and greater efficiency.

PULSED RADAR - S BAND 2-4 GHz.

CURRENT POWER 12 kW FUTURE 20 kW 224 TRANSISTORS WITH HYBRID, RADIAL AND WAVE GUIDE COMBINERS

T/R MODULES ACTIVE APERTURE RADAR 8 - 12 GHz

CURRENT POWER 8 W FUTURE 20 W

MISSILE SEEKER Ka BAND

CURRENT POWER 3 W FUTURE 10 W

SATCOM C BAND 4-6, Ku 12 -14 GHz

C BAND: CURRENT POWER 50 W FUTURE 100 W

Ku BAND: CURRENT POWER 25 W FUTURE 50 W

E/W SYSTEMS

I/J BAND: CURRENT POWER 2 W FUTURE 5 W

APPENDIX D

BIPOLAR JUNCTION POWER TRANSISTOR CHARACTERISTICS

STEPHEN P. JACHIM

Introduction

This report describes some of the fundamental operational characteristics of bipolar junction power transistors in relation to various classes of operation for these devices. A discussion of the behaviors and limitations typically associated with power devices is given first. This is followed by a development of the stresses placed on devices under various operating conditions.

High-Power Device Characteristics

Bipolar junction transistors (BJTs) designed for use in high-power applications are optimized for operation in the environments associated with these applications. In general, these environments can be characterized as high-voltage, high-current and high-dissipation regimes. Figure 1 shows the approximate locations of these regimes on a typical device collector characteristic in the common-base configuration. The specific stresses experienced by a device are determined by the detailed trajectory taken by the intrinsic device through this characteristic as a function of

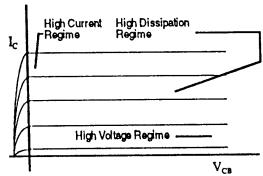


Figure 1. Operating regimes.

time. This trajectory is a function of the device itself, the circuit in which it operates and the drive signals that are applied to it.

The upper limit of the high-voltage regime is determined either by avalanche breakdown of the base-collector junction or by punchthrough. Avalanche breakdown occurs when mobile carriers, under the influence of the collector depletion layer drift field, acquire enough kinetic energy between collisions to generate additional carriers through impact ionization. Punchthrough occurs when the collector depletion layer extends all the way through the base to the emitter. Whichever mechanism occurs at the lowest voltage is the limiting one, but modern devices are generally limited by avalanche breakdown. Critical voltages for these phenomena are determined by the specific doping profile and dimensions of the device. Adjustments to the doping densities can increase the breakdown voltage, but must be balanced against the prominence of surface leakage in the collector region and reduced gain. In addition geometrical effects, particularly in planar epitaxial devices, can cause premature reverse breakdown if not carefully managed.

The occurrence of reverse breakdown, either by avalanche or punchthrough, is not by itself detrimental to a device. What can cause damage is the potentially large currents which may flow in the collector under these conditions. This can lead to catastrophic device failure from excessive dissipation in the collector region or from metallization or bond wire failure due to resistive losses. Excursion into these failure modes can occur rapidly and uncontrollably. Therefore, care must be exercised in the design of the embedding circuit if operation in the high-voltage regime is anticipated.

If the device is operated in the common-emitter configuration, another voltage limitation known as the sustaining voltage becomes relevant. The sustaining voltage is that voltage from collector to emitter at which the incremental current gain, β , approaches infinity due to the onset of avalanche in the collector. While a transistor can be, and sometimes is, operated in the avalanche mode beyond the sustaining voltage in switching applications, this is not practical for amplifier circuits. The negative resistance developed by the device in

this regime can interact with the impedance of the output matching circuit, leading to excessive dissipation and rapid device failure. Typically, the sustaining voltage for a given device lies between 40% and 60% of the collector-base avalanche breakdown voltage. This is because avalanche breakdown occurs when the avalanche multiplication factor reaches infinity, while a multiplication factor only slightly greater than one is required to cause a singularity in the common-emitter current gain.

The lower limit of the high-current regime is defined by the onset of high-level injection effects. Such effects become apparent when the concentration of minority carriers injected into the base region becomes comparable to the concentration of majority carriers, which is essentially the same as the donor impurity concentration. High-level injection is manifested by, among other things, a reduction in emitter efficiency and thus current gain. The ultimate upper limit of device current is determined either by excessive dissipation or failure of device metallization or bond wires.

A simplified planar transistor cross section is shown in figure 2. At the relatively high current levels associated with high-level injection, lateral currents in the base, that is those currents parallel to the base-emitter junction, become significant enough to effect the behavior of that forward-biased junction. In essence, the voltage drop produced by currents flowing laterally through the high-resistivity base region reduces the forward voltage applied to the junction near the center of the emitter. The debiasing effect caused by self-crowding in

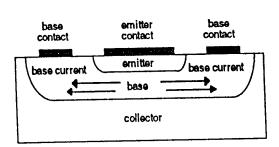


Figure 2. Planar transistor geometry.

the base region significantly reduces the contribution of current injected in the central regions of the emitter to the total emitter current. At very high injection levels, almost all of the emitter current injection occurs at the edges of the emitter. For this reason, the current-handling capacity of bipolar junction power transistors is normally scaled as a function of emitter periphery rather than emitter area.

The emitter capacitance, however, remains a function of emitter area. Thus the frequency response of a power transistor can be improved by choosing an emitter geometry with a high ratio of periphery to area. Many structures have evolved to address this need, such as the overlay, interdigitated and matrix geometries. In practice, however, a tradeoff emerges between improved performance and the complexity of the associated structure. The choice of geometry can also strongly influence the ability to incorporate emitter ballasting as described below.

Because the current injected through the forward-biased emitter-base junction has a positive dependence on temperature, a thermal instability known as hot spots can occur, particularly at high currents. Hot spots can be initiated at crystal defect sites or can appear randomly in a homogeneous crystal. When such a spot forms, emitter current is increasingly concentrated in a small transverse area, increasing the local temperature. Beyond a certain limit, hot spots can become regenerative and if left unchecked, can lead to device failure due to thermally-induced mechanical stress or localized melting of the crystal. Current filamentation of this type is sometimes called forward second breakdown. An effective measure against runaway hot spots is to subdivide the emitter into many small sections, each with an emitter ballasting resistor in series. This resistor is chosen large enough to damp the growth of any anticipated hot spot in each emitter section.

A long-term reliability concern in power devices is electromigration. This phenomenon exhibits itself most prominently in metallic conductors carrying large dc current densities. The momentum transfer between mobile charge carriers and metal ions can cause physical displacement of the thin metal films of a transistor. Changes in any one of several physical parameters associated with a conductor can cause electromigration. For instance, the discontinuity in a conductor traversing the step of a diffusion window can lead to a metallization failure, given enough time.

A detailed discussion of the complex nature of electromigration is beyond the scope of this report [1]. In theory, the mean time to failure for electromigration depends exponentially on an activation energy associated with a particular metal system and inversely with the square of current density. Suffice it to say that one effective means of mitigating this problem is to choose a metal system with a high activation energy, such as gold. Gold by itself cannot be used for metallization as it forms a high-temperature eutectic with silicon, and must be used in conjunction with an underlying barrier metal. For a number of reasons, the added complexity of such compound metal systems can lead to other equally catastrophic long-term failure modes. Certain aluminum metal systems, properly engineered, can exhibit comparable resistance to electromigration while avoiding other failure modes. At some point in the packaging process, however, a transition will usually be made to a gold conductor system. Gold-aluminum intermetallic compounds can form over time which can limit the longevity of a device. Formation of these compounds is accelerated by the elevated temperatures experienced on the surface of a transistor. Thus it is usually preferable to make the transition to gold at a point of low temperature in the package.

The primary dissipation limits are operating junction temperature and second breakdown. The junction temperature has a combined direct dependence on the instantaneous device dissipation, the thermal resistance from the junction to the ultimate heat sink and all intervening thermal time constants. Devices can usually handle short-duration peak power levels much higher than would be allowed continuously due to the thermal time lag of the junction. This time lag also allows the junction temperature for a device operated at RF frequencies to be calculated as a function of the average dissipation over an entire RF period. Care must be exercised, however, to account for quiescent device dissipation when it is not excited by RF.

For silicon devices, the critical junction temperature is about 200° C. Above this temperature, thermal carrier generation significantly degrades transistor action. Temperatures much above 200° C risk irreversible damage to the device. In any case, high junction temperatures have a strong effect on long-term device reliability, as chemical and metallurgical aging mechanisms are greatly accelerated.

Second breakdown primarily occurs at high current-voltage combinations. As discussed before, emitter ballasting greatly improves the resistance of a device to second breakdown. Further protection is usually provided by restrictions to the safe operating area of the device.

Operational Stresses

Figure 3 shows representative collector characteristics for a typical device operated in both the common-base (CB) and common-emitter (CE) configurations. Three major differences

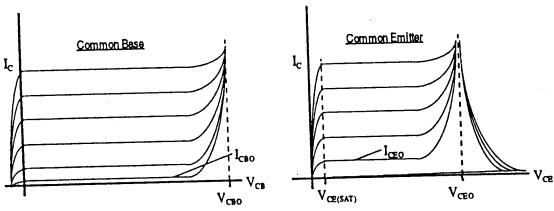
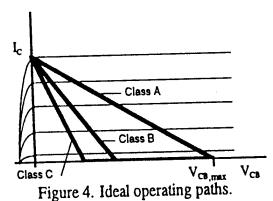


Figure 3. Typical collector characteristics.

in behavior are immediately apparent. First, the high-voltage regimes are characterized by the avalanche breakdown voltage (V_{CBO}) and the sustaining voltage (V_{CEO}) for the CB and CE configurations, respectively. As noted above, V_{CEO} is substantially lower than V_{CBO} . Second, the saturation voltage ($V_{CE(SAT)}$) for the CE configuration is nonzero, while the corresponding value in the CB configuration is essentially zero. And last, the minimum CE collector current (I_{CEO}) is approximately β times larger than the corresponding CB value (I_{CBO}). All three of these differences reduce the ranges of current and voltage achievable in the CE configuration with respect to the CB configuration. Thus the CB configuration is frequently preferred for high-power applications, as it often demonstrates superior output power and collector efficiency.

An objective of a power amplifier design is to establish conditions that coerce the output of an active device to traverse a locus on the device characteristic called the ideal operating path. The actual operating path is determined jointly by the circuit loading the output, by the characteristics of the device itself, and by the stimulus applied to the device. Ideal resistive operating paths for class A, B and C operation are shown superimposed on a typical collector characteristic in figure 4.



Several assumptions are implicit in the use of figure 4 which may or my not be warranted in a particular application. The load is assumed to be resistive, and in practice a resonant load, driven on resonance and in the steady state, well approximates this condition. However, if the load is driven off resonance, transients exist, or significant harmonic energy obtains, the actual device operating path may differ significantly from the ideal load line. Also, complex operating modes such as mixed-mode class C have the potential of producing substantial short-duration departures from an ideal operating path. The load line design is assumed referenced to the intrinsic device terminals, and the parasitics of the device are considered part of the external circuit for analysis purposes. It is also assumed that all energy storage and delay phenomena associated with the intrinsic device can be adequately modelled with lumped reactive components external

to instantaneous intrinsic device junctions. While this assumption is usually supported for devices exhibiting useful behavior at a given frequency, care should be exercised that it not be misapplied in a particular design. Also assumed is that the device output port is free of second-order effects such as base widening. This assumption, while usually appropriate for initial design purposes, should be used with care. Deviations of the operating path from the desired load line can substantially impair the performance of the amplifier and, if significant enough, can lead to device damage.

Because of the differences between the assumed and real behaviors of a device as it is operated in a particular situation, the most valuable method for predicting the operating path of that device is detailed and comprehensive numerical simulation. However, as a practical matter, an initial design is usually pursued on the basis of the above assumptions, followed by fine tuning through simulation. Empirical post-production trimming of an amplifier can optimize against disregarded physical effects and imponderables, but should be limited so as not to depart radically from simulations.

Power amplifier design, like many engineering endeavors, is a complex mix of analysis, assumption and judgment bearing on the characteristics and limitations of the devices used. Care must be taken not to exceed specified maxima of current, voltage and dissipation at all device terminals under all anticipated conditions. For practical design purposes, a safe operating area is defined as a composite of the device limitations, and is superimposed upon the characteristic curves of the device as shown in figure 5. Although the safe operating area cannot precisely represent

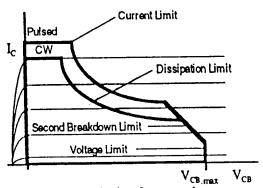


Figure 5. Typical safe operating area.

all device limitations simultaneously, operating paths within the safe operating area will not exceed any specified ratings. Thus the safe operating area is a useful design tool for engineering purposes.

Note in figure 5 that some allowance is given for increased current and/or dissipation under pulsed conditions. The limiting pulse length is defined on the basis of a device-specific critical time period, such as the time lag of junction temperature under transient dissipation conditions. With respect to steady-state CW operation, the collector-base junction can dissipate substantially more power under pulsed operation, but only until the junction temperature reaches its specified limit. Typical time constants for pulsed operation are on the order of 10 to 100 microseconds.

Power transistors are sometimes specified as being appropriate for a specific mode of operation, such as pulsed class C. In reality, of course, all transistors share the same fundamental principles of operation. Therefore, with an appropriate choice of load line and quiescent bias, any device can potentially function in any class of operation. In practice, however, restrictions may be required on the operation of a device in a mode for which it is not optimized.

Several technical factors are relevant to the optimization of devices to specific modes of operation. For the purposes of this discussion, class B operation can be considered to be a limiting case of class C operation. Due to the differences in their operating paths, devices operated in class A are frequently dissipation limited, while devices operated class C are more likely to be voltage and/or current limited. In addition, because the emitter current of devices operated class C derives from the RF input waveform and is thereby fairly uniformly distributed across the emitter structure, thermal stability is of somewhat less

concern under this condition. The quiescent current in devices operated class A, however, does not benefit from such a distribution mechanism, and must rely on other techniques for thermal stabilization. Emitter ballasting can thus be fundamentally important to stable class A operation. But in any case, perturbations of the actual operating path due to such effects as load mismatch, transients and harmonics prescribe significant emitter ballasting for all power BJTs in order to increase their robustness against damage in nonideal situations.

Inherent device linearity, gain, or efficiency may also suit a given device to a particular mode of operation. In many cases, linearity is an important design objective for devices designed for class A or AB operation. This may drive the device design to incorporate copious emitter ballasting beyond that required for thermal stability, even to the point of significant gain and efficiency degradation.

The design of the epitaxial layer of a power BJT is necessarily a compromise based on the intended use of the device [2]. Linearity in the high-current regime requires a high space charge limit for current in the collector depletion layer, which in turn requires a relatively high doping density. This is in conflict, however, with a requirement for high avalanche breakdown voltage, as this requires a relatively low doping density [3]. In order to maximize gain, power and efficiency for a BJT, the epitaxial layer is kept as thin as possible. The collector may even be fully depleted during operation. Countering this design choice is the desire for increased robustness of the device. Residual resistance in an undepleted collector will provide fairly uniform spreading of any avalanche breakdown current. In the depleted condition, however, only space charge effects provide any measure of current spreading. Space charge induced spreading only works over a limited voltage range, and once this range is exceeded, avalanche injection second breakdown occurs, often leading to device damage.

Because it requires a larger input drive signal, a device operated class C will exhibit several dB less gain than when operated class A. The impact of this gain reduction on the power-added efficiency of an amplifier should be assessed. Also, the emitter-base junction of a device operated class C will be more highly stressed than in class A, as it is reverse biased during a portion of the RF cycle.

Having said all that, however, many times the specification of a device for a particular class of operation is actually driven in part by marketing considerations. For instance, assume a substantial market is discerned for an application which utilizes, for efficiency reasons, a class C output stage. An example might be airborne DME transponders. A transistor which might otherwise be useful in a class B, or perhaps even a class A, application will be labeled as a class C device for the target market. The utility of a particular device to a specific application is best assessed in light of the considerations discussed above, with less emphasis placed on a manufacturer's label. In fact, it appears that the current trend of some major device manufacturers is away from application-specific device specification.

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APPENDIX E REPORT ON COLLECTOR MODULATION

FRANK CASSARA

Collector Modulation

A practical circuit for collector modulation is illustrated in Fig. 1.

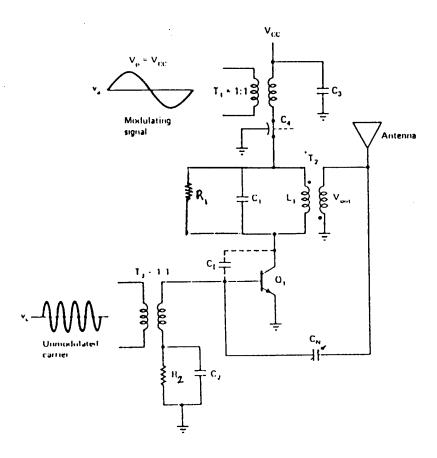


Fig. 1 Schematic diagram of collector modulator.

Its principle of operation can be described as follows. The transistor is driven from cutoff to saturation with the unmodulated carrier excitation signal applied to the base. When the transistor is in saturation its peak collector current is determined by the instantaneous value of the supply voltage $V_{cc} + v_a$ and not by the base driving signal. v_a denotes the baseband modulating waveform. Hence the collector current flows in a train of narrow pulses with peak amplitude proportional to v_a as illustrated in Fig. 2.

The parallel $R_1L_1C_1$ tuned circuit is designed to resonate at the carrier frequency. If its Q is sufficiently high its bandwidth is narrow and the harmonics in the collector current will not contribute significantly to the voltage across the tuned circuit and hence the antenna output voltage appears as in Fig. 2 provided the maximum frequency of the modulating waveform is less than the 3 dB bandwidth of the tuned circuits.

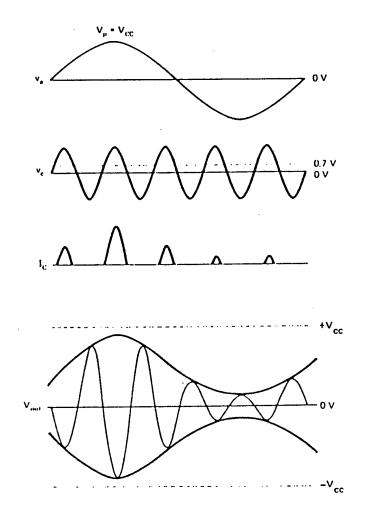


Fig. 2 Collector modulator waveforms.

 R_2 serves a base bias resistor, and can adjust operation from Class B thru Class C (for highest efficiency). If the peak value of v_2 equals V_{cc} , 100% AM modulation index is achieved. C_3 is a power supply decoupling capacitor and behaves as an ac short (even at the modulating waveform frequencies) and prevents ac signals from entering the V_{cc} dc power supply.

 $C_{\rm I}$ represents the transistor's internal parasitic base-collector capacitance and may cause instabilities at some frequency. $C_{\rm N}$ is, therefore, inserted to serve as a neutralizing capacitor to cancel the collector signal fed back to the base through $C_{\rm I}$. C_4 is an RF bypass capacitor. It is designed to behave as a short at the relatively high RF carrier frequency but is an open circuit at the modulating frequency. It thus prevents any RF from reaching either the dc power supply or the modulating waveform source. Collector modulation, therefore, allows for linear envelope modulation (double-sideband AM) at high power levels.

Efficiency Analysis

The Fourier series expansion of the collector current's periodic pulse train is given by

$$i_c = I_p[b_0 + b_1 \cos \omega_0 t + b_2 \cos 2 \omega_0 t + \cdots]$$

where,

$$I_{p} = \frac{[V_{cc} + v_{g}(t)]}{R_{1}}$$

For Class B operation, the Fourier series coefficients reduce to

$$b_0 = \frac{1}{\pi}$$

$$b_1 = \frac{1}{2}$$

$$P_{dc} = \overline{I_{supply}} \ V_{cc} = \overline{I_c} \ V_{cc} = \frac{I_p}{\pi} \ V_{cc} = \frac{[V_{cc} + V_a(t)]}{\pi R_1} \ V_{cc}$$

where the bar denotes average value.

Assuming $\overline{v_a(t)} = 0$,

$$P_{dc} = \frac{V_{cc}^2}{\pi R_1}$$

$$P_{ac} = \frac{1}{i c_{c, fund}^2} R_1 = I_p^2 \left(\frac{1}{2}\right)^2 \frac{1}{\cos^2 \omega_o t} R_1 = \frac{\left[V_{cc}^2 + 2V_{cc} v_a(t) + v_a^2\right]}{R_1^2} \left(\frac{1}{8}\right) R_1$$

if $v_a = V_{cc} \cos \omega_0 t$ (i.e., 100% AM modulation index) we obtain

$$\overline{v_2} = 0$$

and

$$\frac{1}{v_a^2(t)} = \frac{V_{cc}^2}{2}$$

Hence,

$$P_{ac} = \frac{3}{16} \frac{V_{cc}^2}{R_1}$$

The collector efficiency $\eta = \frac{P_{ac}}{P_{dc}} = \frac{3\pi}{16} = 59\%$

Vestigial Sideband AM

 V_{out} in Fig. 1 is proportional to the product of $(i_c) \cdot (Z_1)$ where Z_1 represents the $R_1L_1C_1$ collector tuned circuit. If the resonant frequency of Z_1 equals the fundamental frequency of the collector current then V_{out} reduces to the double sideband AM signal (illustrated in Fig. 2),

$$V_{out} = n I_p b_1 R_1 \cos \omega_0 t = n V_{cc} \left[1 + \frac{v_a(t)}{V_{cc}} \right] b_1 \cos \omega_0 t$$

where n denotes the transformer ratio and the 3 dB bandwidth of the RLC is assumed larger than the maximum modulation frequency.

If the resonant frequency $\left(\frac{1}{\sqrt{L_1C_1}}\right)$ of the tuned circuit is designed to be <u>offset</u> from ω_0 then the parallel RLC can filter part of the lower or upper sideband of i_c and generate vestigial sideband AM (VSB).

APPENDIX F

LINEARITY OF CLASS C PUSH-PULL POWER AMPLIFIERS

STEPHEN P. JACHIM

Introduction

This report calculates the approximate linearity to be expected from a push-pull class C power amplifier with a narrowband resonant output load. A general description of the theory and methodology utilized is discussed first, along with a description of the nonlinear model used for subsequent analyses. This is followed by calculations of linearity under various conditions of bias and drive level. This is followed by discussion of some techniques to improve the linearity of an amplifier.

Theory of Analysis

The linearity of a transmission component, such as an amplifier, can be characterized in a number of ways. Harmonic distortion is used to describe linearity under single-tone excitation. This linearity measure is useful for broadband amplifiers with CW drive, but does not directly address intermodulation distortion in a narrowband amplifier.

Signals of at least two frequencies must be applied to a device in order to study its intermodulation properties. The behavior of a nonlinear device without memory (i.e., instantaneous) can be expressed as a power series in the independent variable:

$$v_{out}(t) = a + bv_{in} + cv_{in}^2 + dv_{in}^3 + \dots$$

Now if two sinusoids are added to form the independent variable,

$$v_{in}(t) = A \cdot \cos(\omega_A t) + B \cdot \cos(\omega_B t),$$

then the output function can be determined from the series expansion. For this discussion, the series is assumed negligible beyond the cubic term.

$$v_{out}(t) = \left[a + \frac{cA^2}{2} + \frac{cB^2}{2}\right] + \left[bA + \frac{3dA^3}{4} + \frac{3dAB^2}{2}\right] \cos(\omega_A t) + \left[bB + \frac{3dB^3}{4} + \frac{3dA^2B}{2}\right] \cos(\omega_B t) + \left[\frac{cA^2}{2}\right] \cos(2\omega_A t) + \left[\frac{cB^2}{2}\right] \cos(2\omega_B t) + \left[\frac{dA^3}{4}\right] \cos(3\omega_A t) + \left[\frac{dB^3}{4}\right] \cos(3\omega_B t) + \left[cAB\right] \cos((\omega_A - \omega_B)t) + \left[cAB\right] \cos((\omega_A + \omega_B)t) + \left[\frac{3dA^2B}{4}\right] \cos((2\omega_A - \omega_B)t) + \left[\frac{3dA^2B}{4}\right] \cos((2\omega_A + \omega_B)t) + \left[\frac{3dAB^2}{4}\right] \cos((2\omega_B - \omega_A)t) + \left[\frac{3dAB^2}{4}\right] \cos((2\omega_B + \omega_A)t)$$

Several consequences of nonlinearity are apparent from this expression. First, the output amplitudes at dc, ω_A and ω_B now include nonlinear dependencies on the input signal amplitudes. This leads to shifts in the bias point of the active device as well as apparent gain compression and/or expansion at high signal levels.

Harmonics of the input frequencies also appear in the output spectrum. The amplitudes of these components determine the level of harmonic distortion present in the system. Of greater interest here are the terms at frequencies

$$m \cdot \omega_A \pm n \cdot \omega_B$$
.

Terms of this type are called intermodulation (IM) products. The order of an IM product is the index of frequency terms that make up that product, that is m+n. Terms such as

$$2\omega_A$$
, $(\omega_A \pm \omega_B)$

are called second-order terms, while

$$3\omega_B,(2\omega_A\pm\omega_B)$$

are third-order terms.

Now if the amplifier under consideration is narrowband in nature, then the only IM components that are of practical interest are at

$$2\omega_A - \omega_B$$
 and $2\omega_B - \omega_A$.

Because the two input frequencies are close together in frequency, these intermodulation products will likely fall back within the response bandwidth of the amplifier. None of the other nonlinear components will pass through the bandlimited amplifier output. While this analysis was limited to third-order nonlinearities, it can be shown that all odd-order nonlinearities can produce IM components which may fall in the passband of a narrowband device. Therefore odd-order nonlinearities are of primary interest in narrowband systems.

The instantaneous power-series approach will be used for the purposes of this paper. More involved analyses can be used to find the phase and frequency dependence of intermodulation distortion in the presence of memory, or energy storage effects. However in order to utilize these techniques to their potential it is necessary to obtain accurate estimates of all active device parameters as functions of voltage and current. Detailed knowledge of the behavior of all linear embedding networks over frequency are also required. It may be useful to obtain these details in the future, but they are not available to support this work.

Methodology

The approach taken here is to model the most significant instantaneous nonlinear aspects of common-base bipolar junction transistors operated in a class C push-pull amplifier, and then to calculate the response of such an amplifier to a two-tone test signal. Other nonlinear mechanisms, such as the voltage dependence of collector capacitance are neglected here. Intermodulation distortion is computed as a function of signal power. Only third-order IM tones that fall in the passband will be computed.

Two nonlinear effects are considered: the emitter current turn-on threshold associated with bipolar junctions, and the degradation of emitter injection efficiency experienced at high current levels. Both of these effects are modelled as memoryless nonlinear functions. The input terminal characteristic of a common-base amplifier is the same as that of a junction diode:

$$I_{E} = I_{R} \left(e^{\frac{qV_{BE}}{kT}} - 1 \right),$$

where

 $I_F = \text{emitter current (A)},$

 I_R = reverse saturation current (A),

 V_{RE} = base - emitter voltage (V),

 V_{EO} = emitter bias voltage (V),

q = electronic charge (C),

k = Boltzmann's constant (J/K),

T = temperature (K).

At room temperature, $kT/q \approx 26$ mv. Figure 1 shows the input circuit for a common-base amplifier.

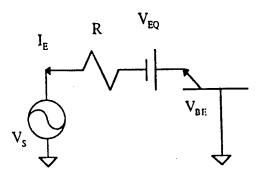


Figure 1. Common-Base Input Circuit.

Using this equation, the source voltage V_s and the emitter current I_E are related through

$$V_S + V_{EQ} + I_E R + \frac{kT}{q} \cdot \ln \left(\frac{I_E}{I_R} + 1 \right) = 0.$$

The root of this transcendental equation, I_E , is found numerically for each value of source voltage. Stimulus by two tones of equal amplitude is expressed by:

$$V_s = V(\cos(2\pi f_1 t) + \cos(2\pi f_2 t)).$$

Assuming the output stage of the amplifier has a center frequency of 800MHz and a bandwidth of 6 MHz, the following choice of frequencies is appropriate:

$$f_1 = 799 \text{ MHz},$$

 $f_2 = 801 \text{ MHz}.$

The resulting IM products of interest will be at

$$f_a = 2f_2 - f_1 = 803$$
 MHz, and $f_b = 2f_1 - f_2 = 797$ MHz.

The collector current I_c is taken as the product of the emitter current and the large-signal emitter efficiency γ :

$$I_C = \gamma \cdot I_E$$
.

For moderately high levels of injection into the base region, emitter efficiency can be approximated as

$$\gamma = \frac{1}{a+b\cdot I_E}.$$

Here, a and b are constants determined from combinations of process parameters for the specific device in question [1]. For the purposes of this analysis, the detailed nature of these process parameters need not be known, as only the dependence of emitter efficiency on emitter current is relevant. In this context, a is taken as the inverse of the small-signal current gain α . The parameter b then determines the magnitude of I_E at which high-level injection effects become apparent. For reliability reasons, transistors usually are not operated at emitter efficiencies less than about 0.8. The properties of the device assumed for this analysis are:

$$\beta = 50,$$
 $R = 0.1\Omega$
 $V_{CBO} = 65 \text{ volts},$
 $I_R = 1 \cdot 10^{-6} \text{ amperes},$
 $I_{C.max} = 22 \text{ amperes},$
 $V_{CC} = 28 \text{ volts}.$

From these the following parameters are derived:

$$a = \frac{1}{\alpha} = \frac{\beta + 1}{\beta} = 1.02,$$

$$b = \frac{\gamma_{\min}}{I_{C,\max}} \left(\frac{1}{\gamma_{\min}} - a \right) = 8.36 \cdot 10^{-3} A^{-1}$$

$$R_{IL} = \text{load-line resistance} = 1.27\Omega.$$

The input power $P_{in,i}$ at frequency f_i is found from

$$P_{\rm in,i} = \frac{{\bf V}_{\rm S,i} {\bf I}_{E,i}^{\bullet}}{2}$$

where bold-faced variables are the associated Fourier coefficients. The output power $P_{out,i}$ is computed as

$$P_{out,i} = \frac{\mathbf{I}_{C,i}^2}{2} \cdot R_{LL}.$$

The total collector current I_{CT} due to the push-pull mode of operation is modelled by subtracting the collector current of the out-of-phase side from current of the in-phase side:

$$I_{CT} = I_{CA} - I_{CB}.$$

Numerical Results

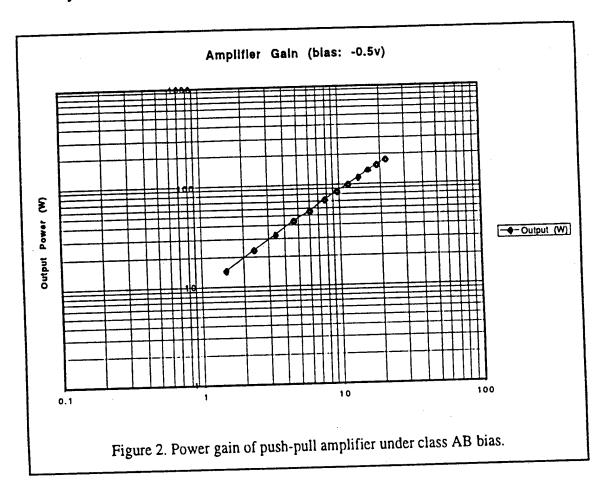
Figures 2 through 7 show the results of the simulations described above. Some immediate observations can be made. The maximum output power for each simulation coincides with operation at the maximum peak current specified for the active device. In each case, the output power achieved is substantially below that expected for a device of this size. This is because the drive waveform, consisting of two independent sinusoids, has a peaking factor of 6dB. Thus, under single-tone stimulation, this amplifier could achieve an approximate output power level from 250W to 350W, depending on biasing.

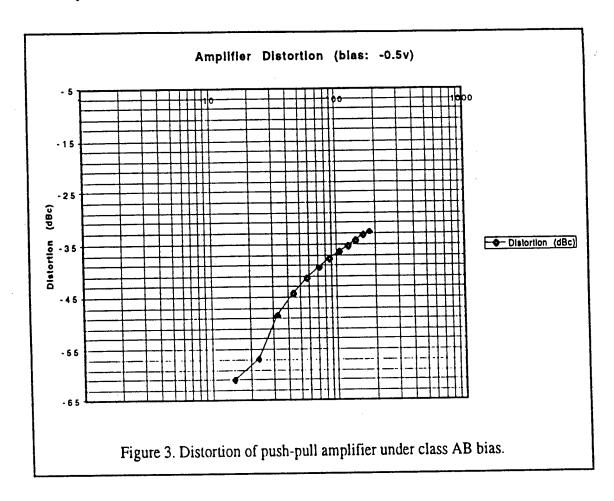
The curves of Figures 2 and 3 result from impressing a slight forward bias on each transistor, overcoming the turn-on potential of the emitter junction. This type of operation is called class AB, as it supports collector current flow during slightly more than 180 degrees of the drive signal. Excellent gain linearity is seen, particularly at low drive levels. At high drive levels, high-level injection effects appear to compress the gain slightly. The intermodulation distortion is plotted in figure 3 in terms of dBc, or dB relative to carrier, and is typical of a device with weak nonlinearities.

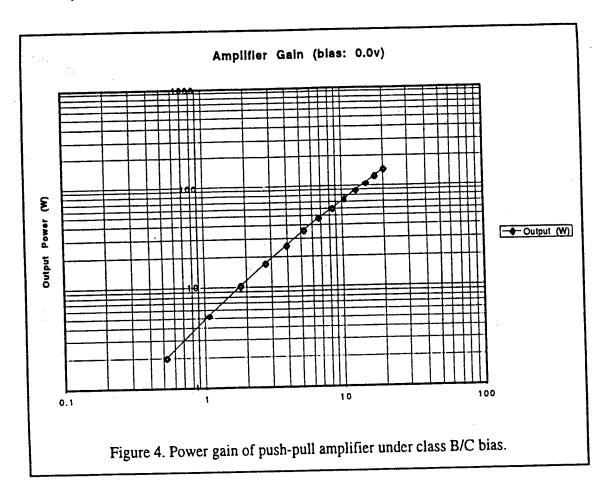
Figures 4 and 5 reflect similar analyses without emitter bias applied. In other words, the emitters have a direct dc path to ground. This is sometimes referred to as class B bias, but in fact is class C operation, hence the class B/C designation. The low-level gain linearity is seen not to be quite as good as the class AB case. This is because of the normal turn-on threshold effect in the emitter circuit. The intermodulation distortion under class B/C bias departs markedly from the class AB case, however. The distortion at low levels differs by several orders of magnitude. The worst distortion appears to occur at signal levels for which the turn-on threshold is most significant [2].

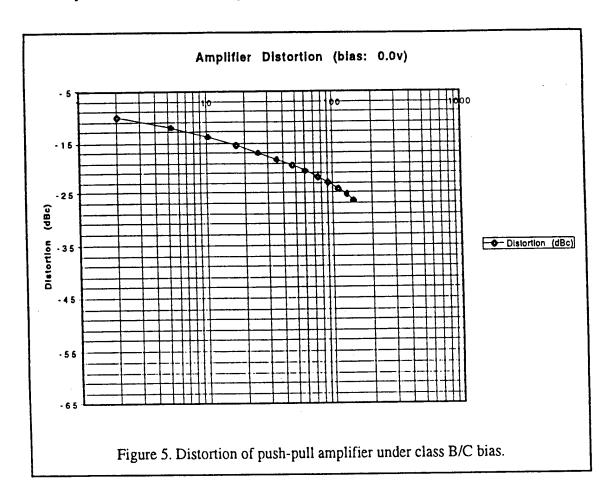
Finally, Figures 6 and 7 reflect simulations under a slight reverse emitter dc bias, corresponding to hard class C operation. Clearly both the low-level gain linearity and intermodulation performance are degraded under this condition.

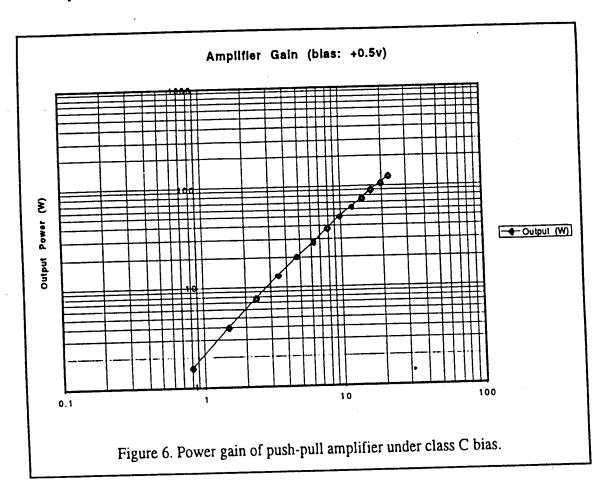
Another general observation is that the maximum output powers under class AB, class B/C and class C operation diminish in the same order. This is because the collector current waveforms become progressively more peaked in shape, therefore delivering less fundamental power under the peak current limitation.

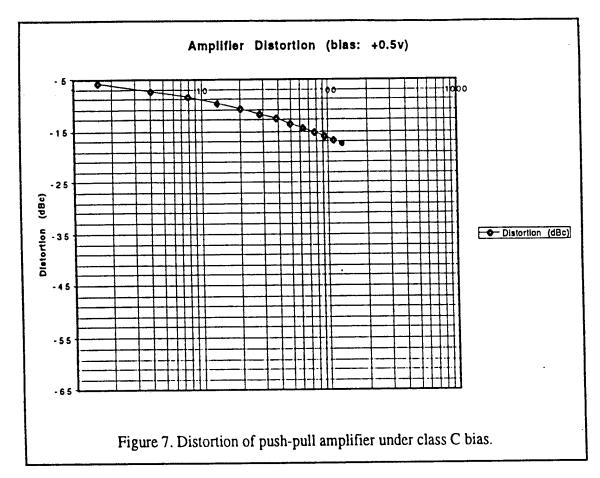












Linearity Enhancement

From the simulations above it appears likely that only the class AB bias case produces distortion low enough to be useful directly in a broadband signal path. Intermodulation distortion caused by this type of weak nonlinearity can be reduced by feedback, feedforward and predistortion techniques [3]. Feedback is not generally used in high-frequency power amplifiers because the bandwidth required for stable operation is difficult to obtain.

Feedforward methods have been used at high frequencies. In this technique, a sample of the power amplifier output signal is attenuated and subtracted from the input signal in such a way as to produce a residual signal consisting of the distortion products of the power amplifier. This residue signal is then amplified separately and subtracted from the power amplifier output, thereby cancelling the distortion. These methods have not been particularly successful, however, because the accuracy and stability required of all components, in particular the power amplifier, is quite difficult to achieve in practice. Variations with temperature and pulse length as well as production variations usually make feedforward cancellation difficult if not impractical.

In the instance of a weak nonlinearity, for example class AB operation, predistortion can provide substantial reductions in intermodulation distortion. This technique consists of deliberately distorting the input signal to the amplifier in such a way as to effectively cancel the distortion produced by the amplifier. For practical purposes, predistortion is often performed at an IF frequency prior to upconversion and application to the amplifier. The distortion improvement achieved depends, of course, on the accuracy with which the predistortion function replicates the distortion in the amplifier. For instance, 20dB of

distortion reduction requires amplitude and phase accuracies of 10 percent and 6 degrees, respectively.

The discussion to this point deals with devices used as linear amplification stages. If the system design and signal format permit, however, other considerations may come in play. Certain digital modulation formats can be achieved by using the amplifier as a high-level modulator. Amplitude states can be defined with collector modulation, analogous to plate modulation in tube amplifiers. Unlike tube amplifiers, however, collector modulation of bipolar junction devices may not be linear in nature because it depends on the saturation characteristics of the device. Joint modulation of the drive signal and collector voltage may be required for linear amplitude modulation [4]. Phase modulation can be applied directly to the amplifier drive signal.

The linearity of direct collector modulation could be improved through nonlinear control of the collector voltage. A device which maps the modulating voltage onto that collector voltage required to produce an overall linear modulation characteristic would serve this purpose. Sophisticated cross-coupled control of amplitude and phase may be required to reduce AM/PM and AM/AM distortion for dense, dynamic modulation formats such as quadrature amplitude modulation (QAM) or distortion-sensitive analog formats like vestigial sideband.

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APPENDIX G

THERMAL ANALYSIS

TOM SCHULTEISS

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Task Description

This task includes analysis of 3 cooling configurations, 2 of which were defined by ARIA microwave. These configurations require cooling of 30, 60 watt transistors embedded in a 14 cm radius aluminum disk. They are located at the 12 cm radius and are evenly distributed around the circumference every 12°. The requirements call for 60 watts of power for each transistor for a total of 1800 watts. The upper limit of temperature of the transistor case is 60 C. The analysis was completed to determine the feasibility of the cooling configurations and set cooling requirements of inlet temperature, flow rate, and pressure drop, for each configuration.

Introduction

ARIA microwave electronics has developed a high power electronic device which requires active cooling. Three cooling options were analyzed to determine flow rate required for each and to determine the maximum temperature of the transistor case. Basic principals of heat transfer suggest that the coolant be directed as close to the heat source as possible to minimize the temperature of the source. Since the high powered transistors penetrate through the disk which they are mounted in, coolant cannot be directed above or below the transistor. The baseline configuration coolant passages are designed as close to the transistors as is practical, The second cooling configuration relies on a large cooling surface, however its effectiveness cannot be fully achieved since the source heat flow is too high for aluminum, and most of the cooling surface is relatively far from the source (transistors). The third configuration, which is not practical, because as I understand the transistor leads must travel through the edge of the disk, however, the results are included to show how this configuration compares to the other two configurations.

Typically a Theta Jc is given for a transistor, representing the case to junction temperature rise, however for this analysis the case temperature was set to 60 C, and analysis was completed for each configuration to show if this temperature limit can be achieved.

Summary

Results of the analysis shows that the baseline configuration, shown in figure 1, results in an acceptable transistor case temperature and also results in pressure drop and flow rate requirements which can readily be achieved. The following table shows the coolant flow and pressure drop requirements as well as the resulting temperature of the case.

Table 1, Flow rate and pressure drop range for baseline cooling configuration

Coolant Flow rate	Pressure Drop	Transistor Case Temperature
gallons/minute	psi	C
.86	3.58	56.8
1.14	6.30	53.6

These results indicate a robust design with respect to coolant flow and resulting transistor case temperature. As will be shown later this is due to a flow rate which is high enough such that the majority of the temperature rise is in the aluminum disk. Therefore, changes in flow rate and pressure drop have secondary effects on the temperature of the case. The disk thermal conductivity is a very important parameter. The type of aluminum was not specified, commercially pure aluminum with a thermal conductivity of at least 125 BTU/HR-FT-°F (AI 1350, 135; AI 1100, 128; AI 6063 126) was assumed for the analysis. If aluminum with this high a thermal conductivity can not be obtained, OFHC copper should be used in its place. OFHC copper has a thermal conductivity of 230 BTU/HR-FT-°F and will result in a high temperature margin.

Thermal grease or an equivalent surface conduction enhancer is required between all mechanically fastened surfaces which transfer the heat between the transistor and the coolant. Without this enhancement the temperature requirements of the transistor can not be met.

Since aluminum was chosen as the disk material, copper can not be used in the coolant loop to pass the water coolant. Since the pressures and flow rates are low, and the temperatures are relatively low, plastic tubes and fittings can be used if aluminum tubes and connections are not practical, this will ensure that no reactions with the aluminum disk will occur. However, using plastic fittings will locally decrease the cooling effectiveness since plastic typically has low thermal conductivity.

Configurations

Figure 1 shows the baseline coolant scheme which considers U shaped tubes/coolant channels that pass around the transistors. A total of 15 U shaped passages cool the 30 transistors.

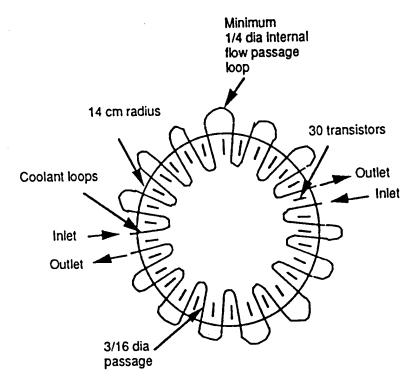


Figure 1, Configuration 1, coolant passages with inlets and outlets.

Of importance in all of these configurations is the mechanically connected surfaces. The high heating rates of the transistors, 60 watts per transistor, would result in unacceptably high temperature rise across these interfaces, shown on figure 2. This can be alleviated with thermal grease, or thermal contact pads. Thermal grease fills in the voids between the surfaces creating a conduction path with enough effective area to limit the local temperature rise to acceptable levels. This is also the most likely problem area since the design calls for 2 screws and heat flow through the plate thickness will tend to curve the plate, tending to open a gap between the surfaces.

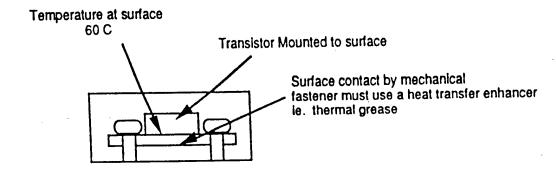


Figure 2, Cross Section showing Transistor and contact surface

Analysis of the cooling scheme includes determining the pressure drop within the coolant loop, the temperature rise of the coolant, the temperature rise within the metal, which also includes any temperature rise across mechanical interfaces. The mechanical interface occurs in all 3 configurations that were analyzed. Figure 3 shows a section representative of one of the coolant channels.

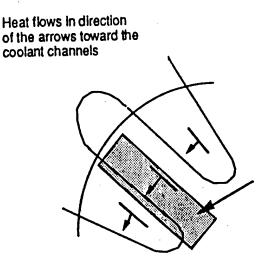


Figure 3, Repeatable section used for analysis

The temperature rise of the coolant is based on the number of resistors cooled by it. Since there are 2 sets of U channels for the disk, one set with 7 channels one set with 8, the one with 8 is used for conservatism. The coolant tubes are formed by internally tapping into the edge of the disk, from the tap, 3/16 round grooves are cut into the disk, they go around each of the transistors as shown in figures 1 and 3.

The other 2 configurations which were analyzed are shown in figures 4 and 5. Figure 4 shows rectangular cooling passages, these passages are very shallow, on the order of 1 mm depth into the page. This is necessary so that the fluid velocity is high enough to obtain good heat transfer across the fluid film.

Table 3, Temperature rise for 30 - 60 watt transistors

ΔT of Coolant C	ΔT Coolant Film C	ΔT Al Disk C	ΔT Plate Interface C	ΔT Connecting Plate C	Temp Of Transistor Case C
8 - 6	6.1 - 4.8	10.5	5.4	6.9	56.8 - 53.6
1.8 - 1.3	4.3 - 3.3	21.5	5.4	6.9	59.9 - 58.4
17	2.4 - 1.8	29.2	5.4	6.9	64.8 - 63.9
	of Coolant C 8 - 6	of Coolant Coolant Film C C 8 - 6 6.1 - 4.8	of Coolant C Coolant Film C C S - 6.1 - 4.8 10.5 1.8 - 1.3 4.3 - 3.3 21.5	of Coolant C Coolant Film C Al Disk C Plate Interface C 8 - 6 6.1 - 4.8 10.5 5.4 1.8 - 1.3 4.3 - 3.3 21.5 5.4	of Coolant C C C C C C C C C C C C C C C C C C C

The results shown above of coolant temperature rise were determined for the flow rates and pressure drop given in table 3. The range of flow rate and pressure drop correspond to the range of coolant temperature rise and film temperature rise given in table 2.

Table 3, Flow rate and pressure drop determined for each cooling configuration

Configuration	ΔP Pressure Drop psi	Flow rate Gallons per Minute GPM
Configuration 1 Figure 1	3.58 - 6.3	.86 - 1.14
Configuration 2 Figure 4	22.5 - 40.9	3.79 - 5.25
Configuration 3 Figure 5	14.8 - 28.1	6.85 - 9.80

Recommendations

The advantage of the baseline configuration is in the proximity of the coolant and the transistors. The closer the heat source is to the coolant the lower the temperature rise. The coolant passages are large enough to pass enough water resulting in low temperature rise of the coolant and low temperature rise across the coolant film to the passage wall. The design also requires low pressure drop and relatively low flow rates, which is desirable.

The importance of thermal grease or a thermal pad can not be overstated in this design. Without thermal grease the temperature rise across the contact surface will increase by a factor of 10 or more, the temperature requirements of the transistor case will not be met.

Certain materials can not be included together in a cooling system that passes water as the coolant. One such set is copper and aluminum, they will corrode in a galvanic cell. Aluminum inlet and outlet feeds can be used, however since the pressure and flow rate required is low, high strength plastic tubing is also acceptable. This suggests that the threaded tapping penetration length on the disk edge be minimized since plastic thermal conductivity is relatively low.

If higher transistor power levels are desired the disk should then be made of copper. The higher thermal conductivity of copper will reduce the temperature rise within the disk, or enable higher power transistors. The inlet and outlet feeds could then be made of copper, locally adding some heat transfer benefit.

Coolant Supply and System

Since the coolant requirements are relatively small (flow rate and pressure drop) reservoir and pumping requirements could be handled by tapping directly into the water supply system of the building. However, if reliability and pressure fluctuations typically found in these type of facilities is unacceptable a reservoir/pump system can be purchased. A preliminary list of pump manufacturers is included. Given flow rate and pressure drop requirements these manufacturers will help in guiding the system that you need. Checking the local yellow pages might also be desirable, this way you can get in touch with a local manufacturer.

P.O. Box 7026, Indianapolis, In 46207-7026 Ph# (317) 924-7380 Fax # (317) 924-7388

942 Memorial Pkwy. Phillipsburg, NJ. 08865 Ph.# 800-847-4041

10 Ruthman Drive/Dry Ridge Kentucky 41035 Ph. # 606-824-5001

P.O. Box 286, Cedarburg Wisconsin 53012 Ph. # 414-377-7000 Ph. # 414-377-7330

This is a very short list which was compiled from Thompsons Registrar and includes pumps manufacture with which my colleagues have dealt with. I'm sure there are local companies that can accommodate the requirements.

References

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- [3] Streeter, V., L., and Wylie, E., B., <u>Fluid Mechanics</u>, McGraw-Hill Book Company, New York, (1975).
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APPENDIX H

P-SPICE UHF POWER AMPLIFIER COMPUTER SIMULATION

JERRY SHMOYS

P-SPICE UHF POWER AMPLIFIER COMPUTER SIMULATION

Introduction

The objective of this study is to examine the effect of paralleling mismatched UHF power transistors on transient and steady state ac amplifier performance. The computer simulation was conducted using P-SPICE. Among the goals of the study include:

- determine if any instabilities occur in the amplifier's response
- determine if any of mismatched transistors cause excessive currents to flow in any of the other transistors.
- determine if there is any degradation in overall amplifier performance
- examine any abnormal behavior in steady state or transient responses.

Matched Transistor Design

The schematic diagram of the amplifier design is illustrated in Fig. 1. It consists of five npn BJT common base transistors connected in parallel. The transistor selected was the SGS-Thomson SD1563 based on its power and frequency specifications. All emitters are connected and driven by a common sinusoidal source. C_1 and L_1 form an input matching network to match the source resistance R_1 to the input impedance of the five parallel emitters for maximum power transfer. All five collectors are connected in parallel and drive the cavity load which is modeled by the series resonant network $R_2L_3C_3$. The output matching network L_2C_2 is designed to match the combined collector impedance to the load at the resonant frequency. The RF choke L_4 behaves as an ac open and dc short to supply V_{cc} bias voltage to all five collectors.

The first simulation conducted models all five transistors identically. Fig. 2 illustrates the sinusoidal steady state ac response of the output load current vs. frequency. As expected we see the resonant bell shaped curve with center frequency of 453 MHz, peak amplitude of 68 amperes, and 3dB bandwidth of 2.5 MHz.

The transient response of the power amplifier is illustrated in Fig. 3 which is a plot of the load current vs. time with a 16V peak-to-peak excitation signal. The rise time of the envelope is approximately 80 nsec which corresponds to the reciprocal of the 3dB bandwidth of the amplifier's low pass equivalent.

The collector currents are identical for the matched transistor case and are illustrated in Fig. 4. They each have an exponentially growing envelope reaching a steady state peak amplitude of 16 Amperes. This falls below the maximum allowed value of 21.6 amperes quoted on the manufacturer's data sheet. The collector voltage is illustrated in Fig. 5 and reaches a peak amplitude of 130 volts which exceeds the maximum allowed. These large voltages are expected since the class C transistor collector currents are rich in harmonics and the series RLC cavity has a high impedance off resonance. This combination will lead to large collector voltages. In practice, this off resonance load impedance will have to be limited to insure these collector voltages remain within safe limits.

The power gain for this design is given by

Power
$$Gain = G_p = \frac{P_{out}}{P_{in}} = \frac{(I_{Load,rms})^2 R_L}{\frac{(V_{in,rms})^2}{R_1}} = \frac{925 \text{ Watts}}{160 \text{ Watts}} = 7.6 dB$$

yielding a collector efficiency of

$$\eta = \frac{P_{ac}}{P_{dc}} = \frac{925 \text{ watts}}{1550 \text{ watts}} = 60\%$$

Mismatched Transistor Design

Next, the five transistors were purposely mismatched to determine what effect that would have on amplifier performance. The schematic diagram appears in Fig. 6 and is identical to Fig. 1 except each transistor has different model parameters and are labeled A through E.

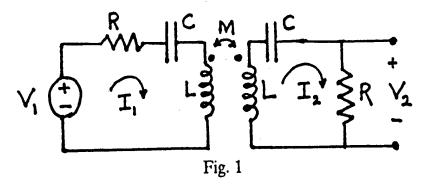
The sinusoidal steady state response is illustrated in Fig. 7. The result is similar to the matched case except the peak amplitude of the load current (I_{R2}) is reduced to 57 Amperes. The resonant frequency and 3dB bandwidth remain essentially the same as the matched case. The total power gain decreased to 6.3 dB and the collector efficiency reduced to 44%.

The transient response of the load current is shown in Fig. 8. The exponential growing envelope reaches a steady state amplitude of 57 Amperes with no instabilities noted. The collector currents for each of the five transistors are illustrated in Fig. 9a-9e for Q_1 thru Q_5 , respectively. All currents fall below the 21.6 Ampere maximum collector current allowed. The common collector voltage appears as in Fig. 10.

The P-SPICE BJT model parameter list is given in Table I. The parameter values used for the mismatched transistors of Fig. 6 are listed in Table II. The variation selected is quite large. For example, transistor current gain (β_F) varies from 10 to 100. Collector junction capacitance (C_{jc}) varies from 50 pF to 200 pF and emitter junction capacitance (C_{je}) varies from 500 pF to 2000 pF. Despite the large variation in transistor parameters chosen for the design example, no instabilities were observed, no transistors exhibited excessively large currents, and no abnormal behavior was observed in any of the steady state or transient responses. In conclusion, mismatched transistors can be paralleled in a UHF power amplifier with no noticeable degradation in performance.

DOUBLE TUNED CIRCUITS

The purpose of this study is to examine the transient response of the double tuned circuit shown below



The loop equations for this circuit are

$$V_1 = (s^2LC + sRC + 1)I_1 - s^2 \alpha LCI_2$$
$$0 = -s^2 \alpha LC I_1 + (s^2LC + RC + 1)I_2$$

where s is the Laplace transform variable and

$$\alpha = M/L$$

Setting $\omega_0^2 = 1/LC$, $Q = \omega_0 L/R$, $x = s/\omega_0$, the transform function V_2/V_1 becomes

$$f_1(x) = \frac{V_2}{V_1} = RI_2 = \frac{(\alpha/Q)x^2}{(x^2 + x/Q + 1)^2 - \alpha^2 x^4}$$

For $\alpha <<1$, Q >>1, the four roots of the denominator are

$$x = -\frac{1}{2O} \pm j(1 \pm \alpha/2)$$

For simplicity we denote the two parameters by

$$a = \alpha/2$$
 and $q = \frac{1}{2Q}$ so that

$$f_1(x) \sim \frac{\alpha}{Q} \frac{x^3}{[x+q-j(1+a)][x+q+j(1+a)][x+q-j(1-a)][x+q+j(1-a)]}$$

We consider two types of input functions:

- 1. Discontinuity in amplitude
- 2. Discontinuity in phase

For the first type of input, we take

$$v_1(t) = V_0 \cos(\omega_0 t) u(t)$$

which has a transform

$$f_2(s) = V_1(s) = \frac{V_0 s}{s^2 + \omega_0^2} = \frac{V_0}{\omega_0} \frac{x}{x^2 + 1}$$

The output transform is then, in terms of x,

$$f(x) \sim A \frac{x^4}{(x+j)(x-j)[x+q-j(1+a)][x+q+j(1+a)][x+q-j(1-a)][x+q+j(1-a)]}$$

where the amplitude factor A is not relevant to the present study. Setting A=1 and expanding f(x) in partial fraction yields

$$f(x) = \frac{R_0}{x-j} + \frac{R_0^*}{x+j} + \frac{R_1}{x+q-j(1+a)} + \frac{R_1^*}{x+q+j(1+a)} + \frac{R_2}{x+q-j(1-a)} + \frac{R_2^*}{x+q+j(1-a)}$$

where the residues are evaluated by the computer. We now evaluate the inverse Laplace transform, remembering that $x=s/\omega_0$, so that the inverse transform of f(x) yields $\bar{f}(\tau)$ where $\tau=\omega_0 t$, or time in radians of the carrier frequency. We get

$$\bar{f}(\tau) = 2Re\{R_0e^{i\tau} + e^{-q\tau}[R_1e^{i(1+a)\tau} + R_2e^{i(1-a)\tau}]\}$$

Denoting by R_{nr} and R_{ni} the real and imaginary parts of R_n , normalized so that the steady state response is of magnitude 1,

$$fn(\tau) = R_{0r}\cos\tau - R_{0i}\sin\tau + e^{-q\tau}[R_{1r}\cos(\tau + a\tau) - R_{1i}\sin(\tau + a\tau) + R_{2r}\cos(\tau - a\tau) - R_{2i}\sin(\tau - a\tau)]$$

Expanding the trigonometric functions of sums and differences, we can write that as

$$fn(\tau) = A(\tau)\cos \tau + B(\tau)\sin \tau$$

where

$$A(\tau) = \{R_{0r} + e^{-q\tau}[(R_{1r} + R_{2r})\cos a\tau - (R_{1i} - R_{2i})\sin a\tau]\}$$

$$B(\tau) = \{-R_{0i} + e^{-q\tau}[-(R_{1i} + R_{2i})\cos a\tau - (R_{1r} - R_{2i}\sin a\tau]\}$$

The envelope of the response is then

$$C(\tau) = [A^2(\tau) + B^2(\tau)]^{1/2}$$

This function is displayed in Figs. 2-7, for Q=100, and coupling coefficient from 0.006 to 0.016, vs. τ in cycles, rather than radians, of the carrier frequency. As is well known the transient lasts about Q cycles and increasing the coupling coefficient speeds up the response at the expense of the increasing overshoot. The "critical" coupling coefficient is 1/Q. We see that, if 10% overshoot is permissible, the coupling coefficient of 1.2Q yields the shortest rise time of about 50 cycles.

For the discontinuity in phase we take the input voltage to be

$$v_1(t) = \sin(\omega_0 t) \qquad t < 0$$
$$= \cos(\omega_0 t) \qquad t > 0$$

or

$$\mathbf{v}_1(t) = \sin(\omega_0 t) + [\cos(\omega_0 t) - \sin(\omega_0 t)] u(t)$$

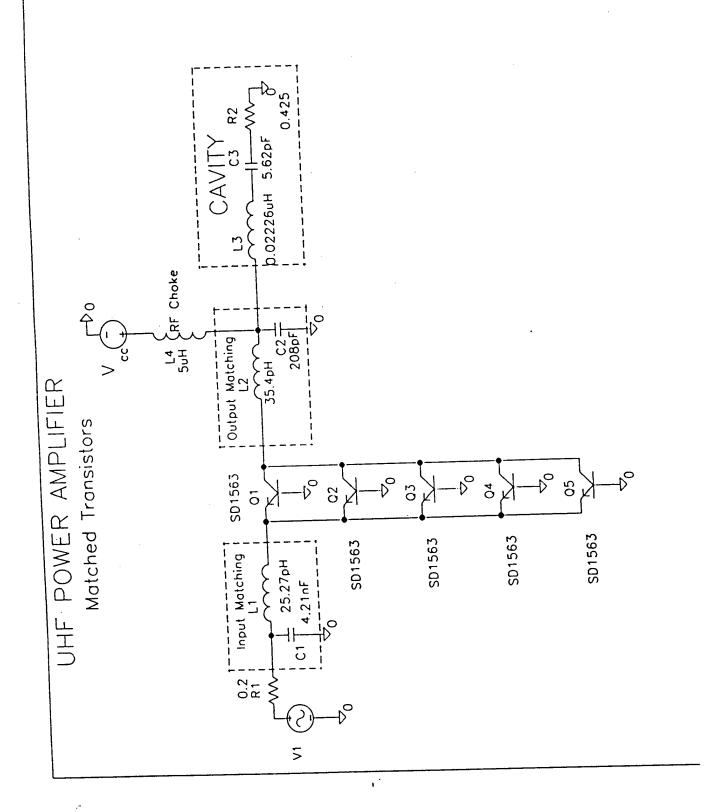
The Laplace transform of the bracketed term is

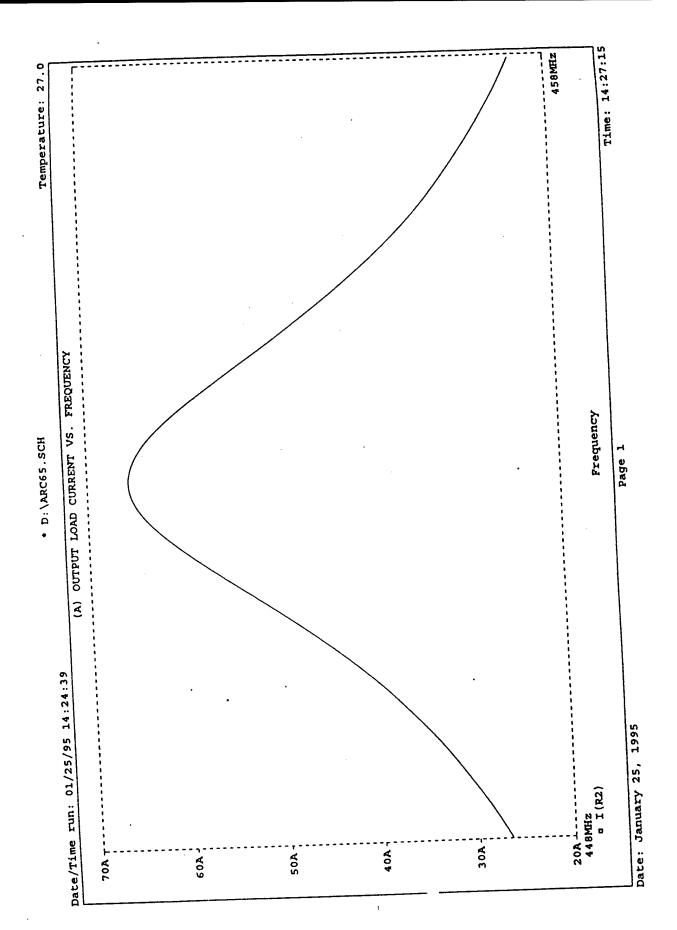
$$\frac{s - \omega_0}{s^2 + \omega_0^2} = \frac{1}{\omega_0} \quad \frac{x - 1}{x^2 + 1}$$

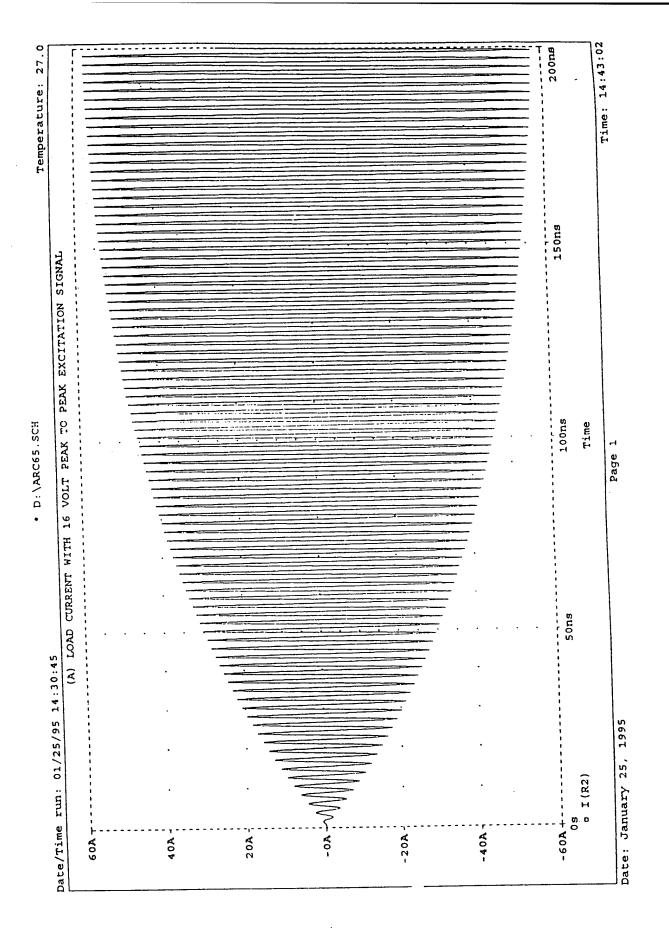
Analysis is the same, except that we have $x^3(x-1)$ in the numerator of the output transform and we have to add $\sin \tau$ to the input. The results, obtained for Q=100 and coupling coefficient 0.006 to 0.018, are similar to those for the amplitude transient. The response is shown on Figs. 8-14, with phase in radians and time in cycles of carrier frequency. It would appear that with phase modulation somewhat higher coupling coefficient might be acceptable, perhaps as large as 1.6/Q, yielding a rise time of about 35 cycles of the carrier.

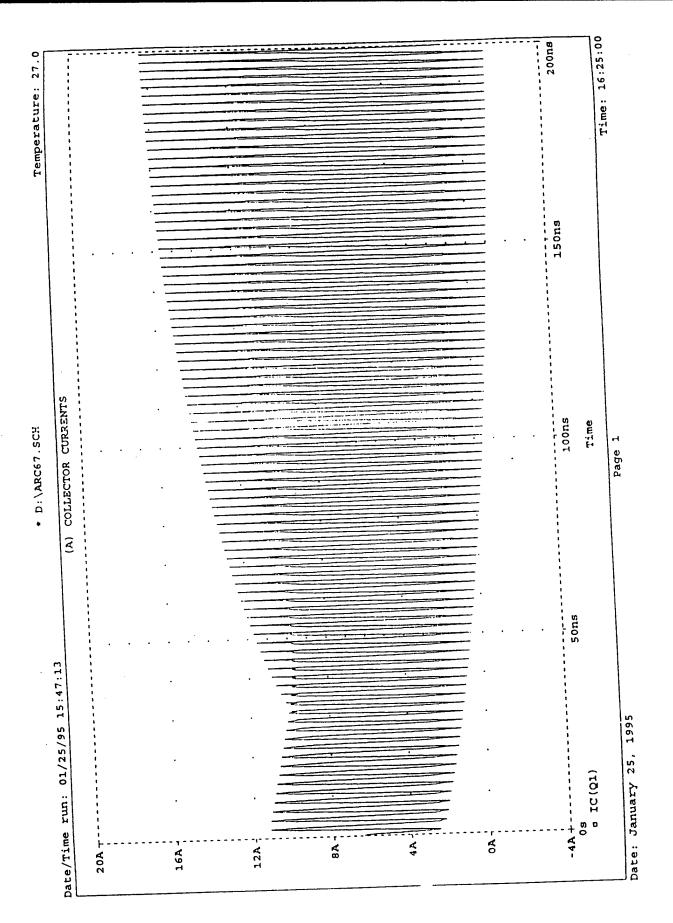
P-SPICE UHF POWER AMPLIFIER SIMULATION

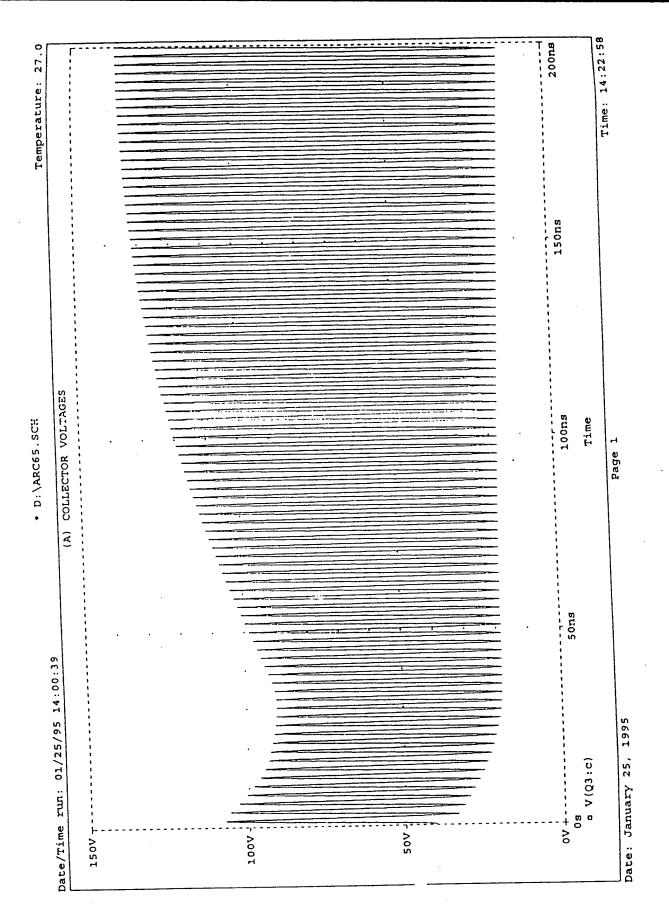
Objective: Examine the effect of paralleling mismatched UHF power transistors on transient and steady state ac performance.





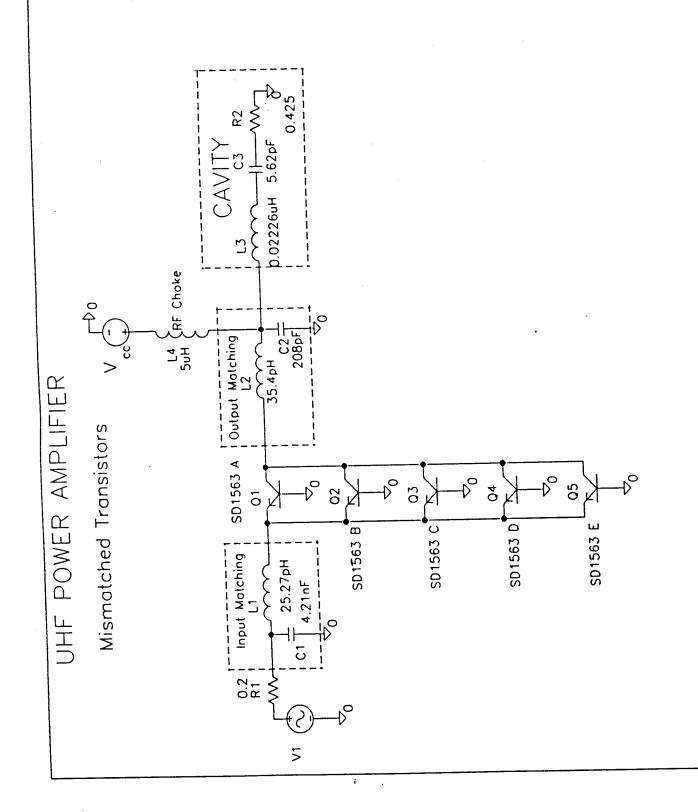


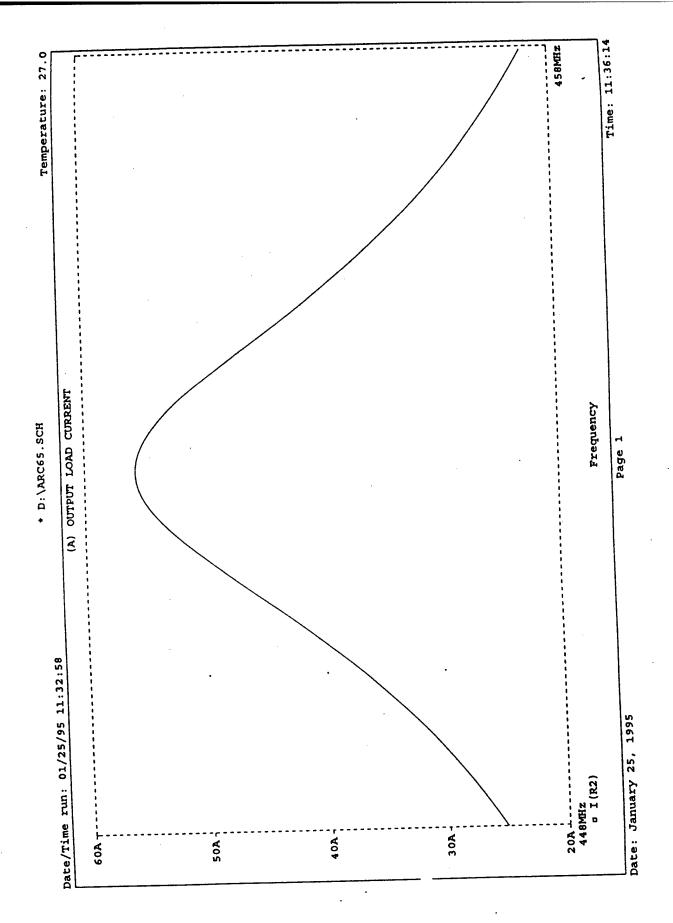


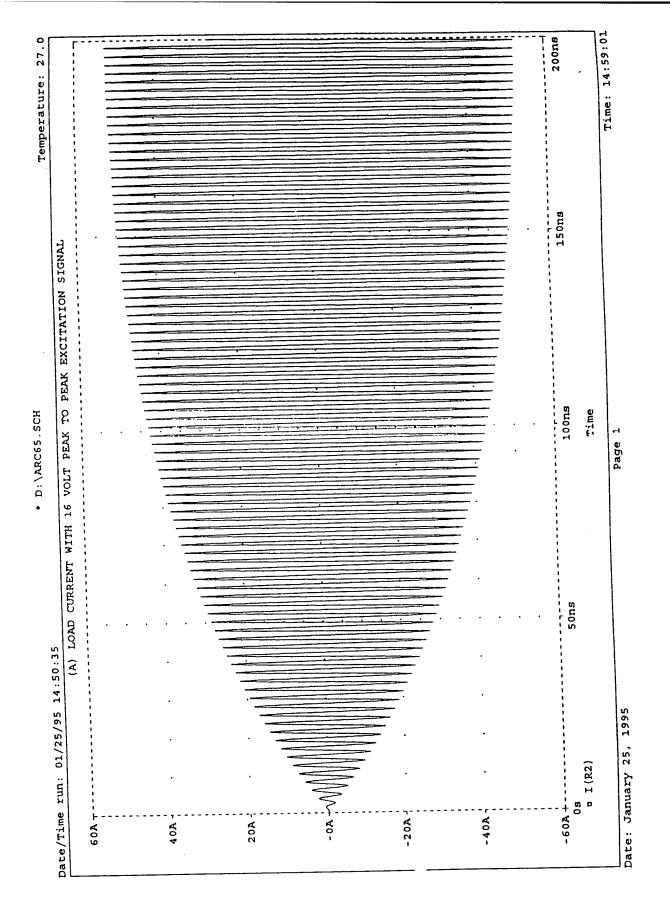


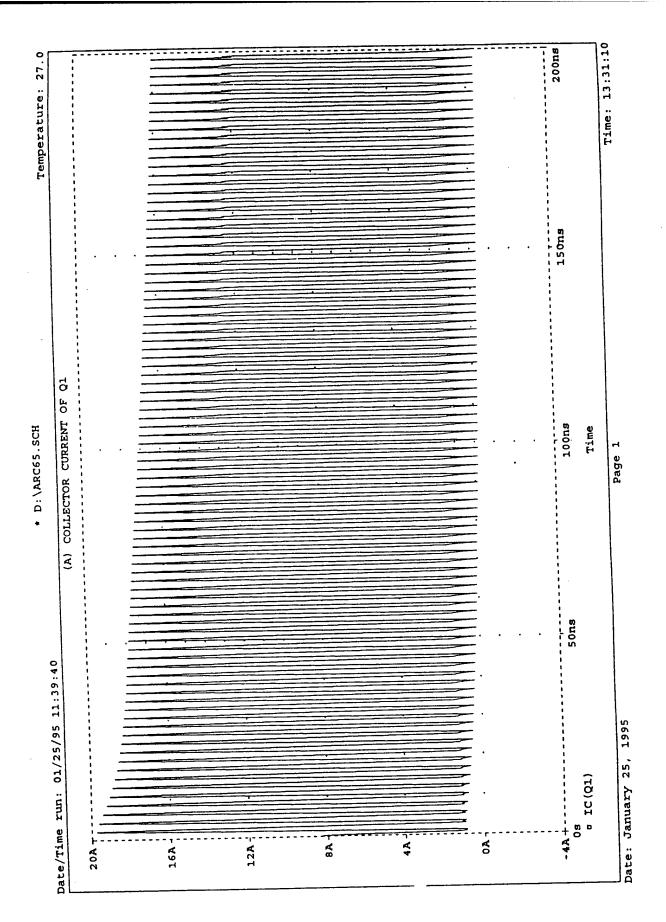
Power Gain =
$$G_p = \frac{P_{out}}{P_{iin}} = \frac{(I_{Load,rms})^2 R_L}{V_{iin,rms})^2} = \frac{925 \text{ watts}}{160 \text{ watts}} = 7.6dB$$

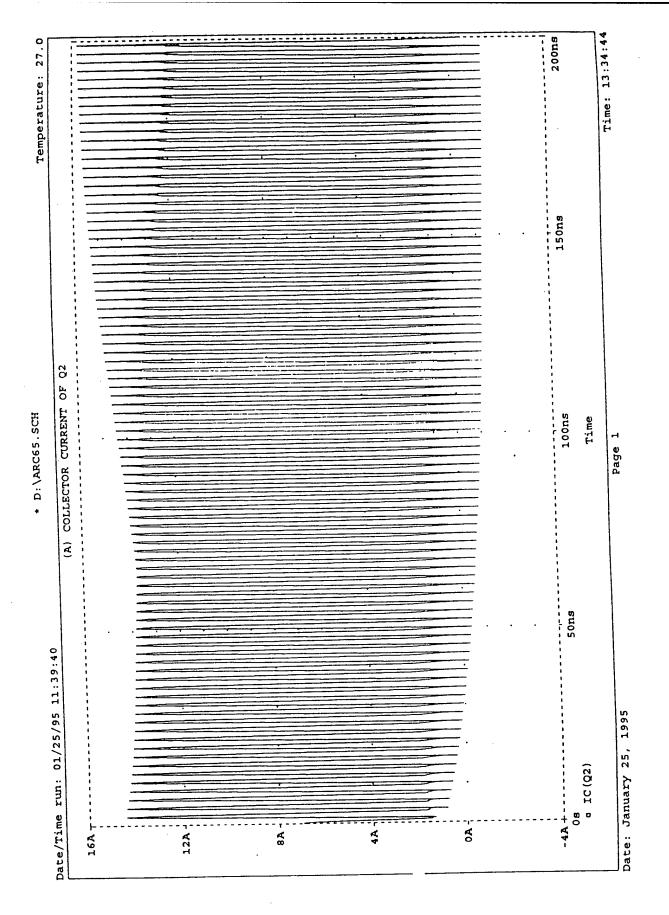
Efficiency =
$$\eta = \frac{P_{ac}}{P_{dc}} = \frac{925 \text{ watts}}{1550 \text{ watts}} = 60\%$$

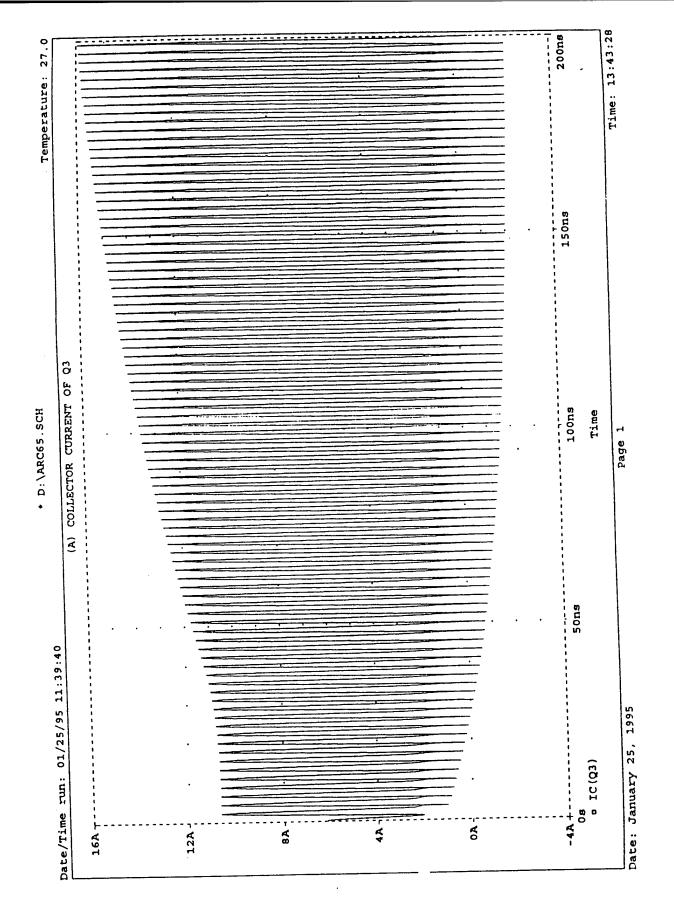


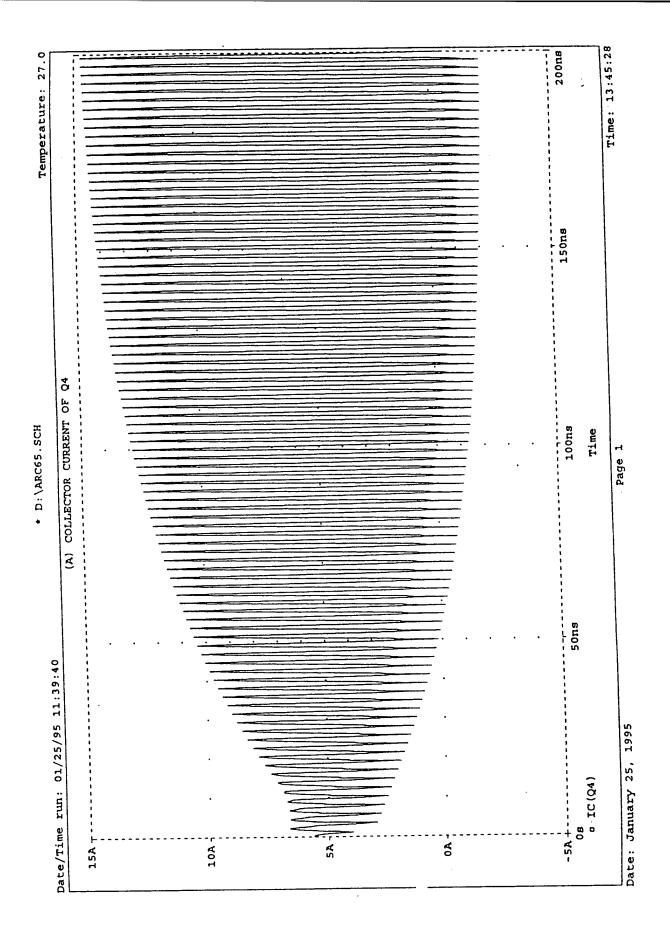


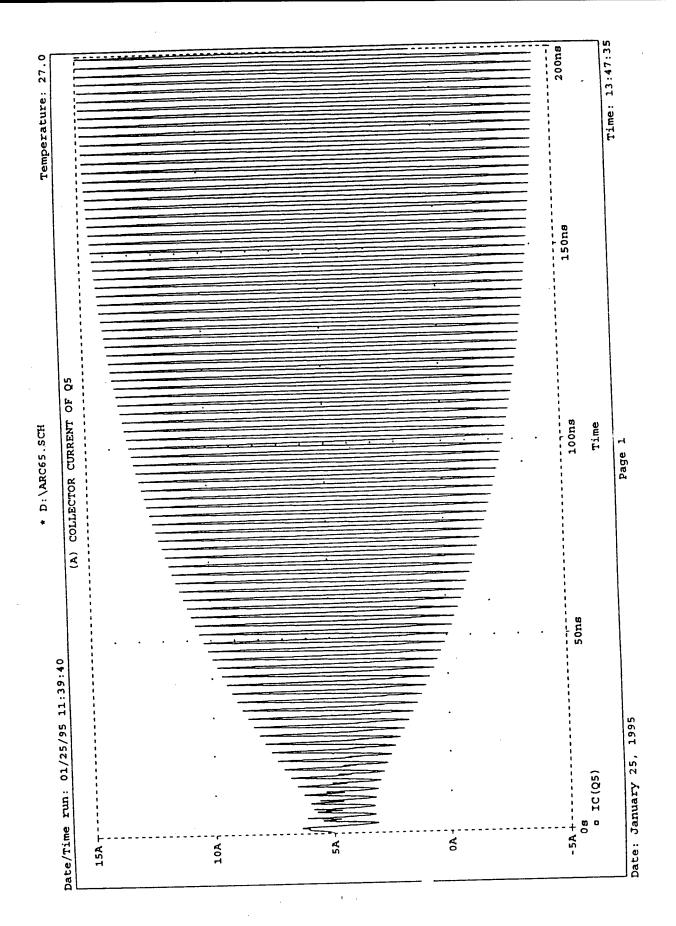


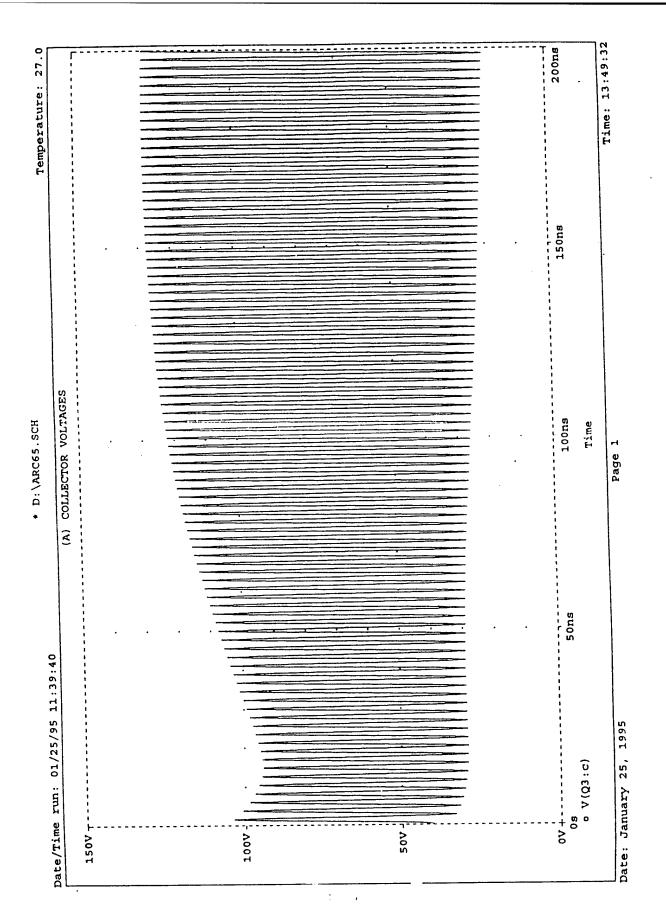












MODEL PARAMETERS OF BJTS

Ideal maximum forward beta 100	Name .	Агеа	Model parameters	Units	Default	Typical
NF Forward current emission coefficient VAF(VA) (KF(IK) VAF(VA) (KF(IK) Corner for forward beta high- current roll-off Base-emitter leakage emission coefficient BR Ideal maximum reverse beta Reverse current emission coefficient VAR(VB) REVERSE Early voltage Volts Reverse current emission coefficient VAR(VB) ISC(C4) Base-collector leakage saturation current NC Base-collector leakage saturation current NC Base-collector leakage emission coefficient NC Base-collector leakage saturation current NC RBM Minimum base resistance Current at which RB falls halfway to RBM RE Emitter ohmic resistance CIE Base-emitter zero-bias p-n capacitance VIE(PE) Base-collector zero-bias p-n capacitance VIE(PE) Base-collector p-n grading factor Fraction of C _b connected internal to R _g CIS(CCS) Collector-substrate built-in potential Base-collector p-n grading factor Fraction of C _b connected internal to R _g CIS(CCS) Collector-substrate built-in potential Base-collector p-n grading factor Fraction of C _b connected internal to R _g CIS(CCS) Collector-substrate built-in potential Base-collector p-n grading factor Fraction of C _b connected internal to R _g CIS(CCS) Collector-substrate built-in potential Base-collector p-n grading factor Fraction of C _b connected internal to R _g CIS(CCS) Collector-substrate built-in potential Base-collector p-n grading factor Fraction of C _b connected internal to R _g CIS(CCS) Collector-substrate built-in potential Base-collector p-n grading factor Fraction of C _b connected internal to R _g CIS(CCS) Collector-substrate built-in potential Base-collector substrate built-in potential Base-collector p-n grading factor Fraction of C _b connected internal to R _g Collector-substrate built-in potential Base-collector substrate built-in pote	IS	•		Amps		
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RBM Minimum base resistance RBM Minimum base resistance RBM Current at which RB falls halfway to RBM RE * Emitter ohmic resistance CJE * Base-emitter zero-bias p-n capacitance CJC * Base-emitter built-in potential CJC * Base-collector built-in potential CJC * Base-collector p-n grading factor CJC * Base-collector p-n grading factor CJC * Base-collector p-n grading factor CJC * Base-collector built-in potential CJC * Base-collector p-n grading factor CJC * Collector-substrate zero-bias p-n CJS(CCS) CJS(CCS) CJS(CCS) COLLECTOR-SUBSTRATE zero-bias p-n CJS(CCS) COLLECTOR-SUBSTRATE p-n grading factor FC Collector-substrate built-in potential CJS(CCS) CJS	NC		Base-collector leakage emission		2	2
RBM Minimum base resistance Ohms RB 100 IRB Current at which RB falls halfway to RBM RE Emitter ohmic resistance Ohms 0 1 RC Collector ohmic resistance Ohms 0 10 RC Collector ohmic resistance Ohms 0 10 RC Base-emitter zero-bias p - n capacitance VJE(PE) Base-emitter built-in potential Volts 0.75 0.75 MJE(ME) Base-emitter p - n grading factor O.33 0.33 CJC Base-collector zero-bias p - n capacitance VJC(PC) Base-collector built-in potential Volts 0.75 0.75 MJC(MC) Base-collector p - n grading factor Farads 0 1P MJC(MC) Base-collector p - n grading factor O.33 0.33 XCJC Fraction of C_{br} connected internal 1 $to R_{b}$ Collector-substrate zero-bias p - n Farads 0 2PF Capacitance VJS(PS) Collector-substrate built-in potential Volts 0.75 MJS(MS) Collector-substrate built-in potential Volts 0.75 MJS(MS) Collector-substrate p - n grading factor FC Forward-bias depletion capacitor Coefficient Volts 0.5 XTF Transit-time bias dependence Coefficient Volts XTF Transit-time dependency on V_{br} Volts XTF Transit-time dependency on I_{cr} Amps 0 PTF Excess phase at $I/(2n^*TF)Hz$ Degrees 0 30° TR Ideal reverse transit time Seconds 0 10NS EG Bandgap voltage (barrier height) Electron-volts 1.11 1.11 XTB Forward and reverse beta temperature-effect exponent Stemperature-effect exponent Coefficient Coeffi	RB	•	Zero-bias (maximum) base resis-	Ohms	0	100
TRB Current at which RB falls halfway to RBM RE	RRM	٠.		Ohms	RB	100
RE Collector ohmic resistance Ohms 0 1 Collector ohmic resistance Ohms 0 10 Collector base-emitter built-in potential Volts 0.75 0.75 MJE(ME) Base-emitter built-in potential Volts 0.33 0.33 Collector built-in potential Volts 0.75 0.75 MJC(MC) Base-collector built-in potential Volts 0.75 0.75 MJC(MC) Base-collector built-in potential Volts 0.75 0.75 MJC(MC) Base-collector p-n grading factor Fraction of Cbc connected internal to RB Collector-substrate zero-bias p-n Farads 0 2PF Collector-substrate built-in potential Volts 0.75 Collector-substrate built-in potential to RB MJS(MS) Collector-substrate built-in potential Volts 0.75 Collector-substrate p-n grading factor Coefficient Volts 0.75 Tollector-substrate p-n grading factor Coefficient Volts 0.75 Transit-time bias depletion capacitor coefficient Volts 0.5 Coefficient Volts 0.75 Transit-time dependency on Vbc Volts 0.5 Coefficient Volts 0.75 Transit-time dependency on Vbc Volts 0.5 Coefficient Volts 0.75 Collector-substrate p-n grading factor Volts 0.5 Collector-substrate p-n grading factor Volts 0.75 Collector-substrate p-n grading factor 0.5 Collector-substrate p-n grading factor 0.5 Collector-substrate p-n grading 0 Transit-time dependency on Vbc Volts 0.75 Collector-substrate p-n grading 0 Transit-time dependency on Vbc 0.5 Collector-substrate p-n grading 0 Transit-time dependency on Vbc 0.5 Collector-substrate p-n grading 0 Transit-time dependency on Vbc 0.5 Collector-substrate p-n grading 0 Tollector-substrate p-n grading 1 Tollecto	IRB		Current at which RB falls halfway			
RC * Collector ohmic resistance CJE * Base-emitter zero-bias p - n capacitance VJE(PE) Base-emitter built-in potential WJE(ME) Base-emitter p - n grading factor VJC(PC) Base-collector zero-bias p - n capacitance VJC(MC) Base-collector built-in potential Volts 0.75 0.75 MJC(MC) Base-collector built-in potential Volts 0.75 0.75 MJC(MC) Base-collector p - n grading factor XCJC Fraction of C_{bc} connected internal to R_{B} CJS(CCS) Collector-substrate zero-bias p - n Farads 0 2PF capacitance VJS(PS) Collector-substrate built-in potential MJS(MS) Collector-substrate p - n grading factor FC Forward-bias depletion capacitor coefficient TF Ideal forward transit time Seconds 0 0.1NS XTF Transit-time bias dependence coefficient VTF Transit-time dependency on V_{bc} Volts ∞ TTF Transit-time dependency on I_{cc} Amps 0 PTF Excess phase at $I/(2\pi^*\text{TF})\text{Hz}$ Degrees 0 30° TR Ideal reverse transit time Seconds 0 10NS EG Bandgap voltage (barrier height) XTB Forward and reverse beta temperature-coefficient IS temperature-effect exponent KF Flicker noise coefficient 0 6.6E—	DE	٠		Ohms	0	1
CJE * Base-emitter zero-bias p - n capacitance VJE(PE) Base-emitter built-in potential Volts 0.75 0.75 MJE(ME) Base-emitter p - n grading factor 0.33 0.33 CJC * Base-collector zero-bias p - n capacitance VJC(PC) Base-collector built-in potential Volts 0.75 0.75 MJC(MC) Base-collector p - n grading factor Volts 0.75 0.75 MJC(MC) Base-collector p - n grading factor p -					_	
VJE(PE)Base-emitter built-in potentialVolts 0.75 0.75 MJE(ME)Base-collector pn grading factor 0.33 0.33 CJCBase-collector zero-bias pn capacitanceFarads 0 $1P$ VJC(PC)Base-collector built-in potentialVolts 0.75 0.75 MJC(MC)Base-collector pn grading factor 0.33 0.33 XCJCFraction of C_{bc} connected internal to R_{B} 0.33 0.33 CJS(CCS)Collector-substrate zero-bias $p-n$ capacitanceFarads 0 0.33 VJS(PS)Collector-substrate built-in potentialVolts 0.75 MJS(MS)Collector-substrate $p-n$ grading factor 0.75 0.75 FCForward-bias depletion capacitor coefficient 0.5 0.5 TFIdeal forward transit timeSeconds 0 $0.1NS$ XTFTransit-time bias dependence coefficient 0.5 0.5 VTFTransit-time dependency on I_{c} 0.5 0.5 TTFExcess phase at $1/(2\pi^*TF)Hz$ 0.5 0.5 TRIdeal reverse transit time 0.5 0.5 EGBandgap voltage (barrier height) 0.5 0.5 XTI(PT)IS temperature-effect exponent 0.5 0.5 KFFlicker noise coefficient 0.5 0.5	CJE		Base-emitter zero-bias p-n capaci-		-	
MJE(ME) Base-emitter $p \cdot n$ grading factor CJC Base-collector zero-bias $p \cdot n$ capacitance VJC(PC) Base-collector built-in potential Volts DAGGE MJC(MC) Base-collector $p \cdot n$ grading factor TFraction of C_{br} connected internal to R_{B} CJS(CCS) Collector-substrate zero-bias $p \cdot n$ capacitance VJS(PS) Collector-substrate built-in potential MJS(MS) Collector-substrate $p \cdot n$ grading factor FC Forward-bias depletion capacitor coefficient TF Ideal forward transit time Seconds VJF Transit-time bias dependence coefficient VTF Transit-time dependency on V_{br} TTF Transit-time dependency on I_r Amps O Degrees O TR Ideal reverse transit time Seconds Daggees O Seconds Seconds O S	VIE(PE)			Volts	0.75	0.75
CJC* Base-collector zero-bias p - n capacitanceFarads01PVJC(PC)Base-collector built-in potentialVolts0.750.75MJC(MC)Base-collector p - n grading factor0.330.330.33XCJCFraction of C_{bc} connected internal to R_{B} 00.330.33CJS(CCS)Collector-substrate zero-bias p - n capacitanceFarads02PFVJS(PS)Collector-substrate built-in potentialVolts0.75MJS(MS)Collector-substrate p - n grading factor00.75FCForward-bias depletion capacitor coefficient0.50.5TFIdeal forward transit timeSeconds00.1NSXTFTransit-time bias dependence coefficient00.1NSVTFTransit-time dependency on I_c Volts x TTFTransit-time dependency on I_c Volts x TTRIdeal reverse transit timeSeconds010NSEGBandgap voltage (barrier height)Seconds010NSXTI(PT)IS temperature-effect exponent31.111.11KFFlicker noise coefficient06.6E-1			Base-emitter p-n grading factor	0.33	0.33	
VJC(PC)Base-collector built-in potential MJC(MC)Volts Base-collector $p-n$ grading factor to R_B Volts 0.330.75 0.33XCJCFraction of C_{bc} connected internal to R_B 02PFCJS(CCS)Collector-substrate zero-bias $p-n$ capacitanceFarads02PFVJS(PS)Collector-substrate built-in poten- tialVolts0.75MJS(MS)Collector-substrate $p-n$ grading factor00.75FCForward-bias depletion capacitor coefficient0.5TFIdeal forward transit timeSeconds00.1NSXTFTransit-time bias dependence coefficient00.1NSVTFTransit-time dependency on V_{bc} Transit-time dependency on I_c Excess phase at $1/(2\pi^*TF)Hz$ TR Ideal reverse transit timeDegrees Seconds Seconds Degrees030°TRIdeal reverse transit time Bandgap voltage (barrier height) Transit-time coefficientSeconds Seconds Degrees1.111.11XTI(PT)IS temperature-effect exponent Flicker noise coefficient36.6E-	CJC	•	Base-collector zero-bias p-n ca-	Farads	0	1P
MJC(MC) MJC(MC) MJC(MC) MJC(MC) Fraction of C_{br} connected internal to R_B CJS(CCS) Collector-substrate zero-bias p - n capacitance VJS(PS) Collector-substrate built-in potential MJS(MS) Collector-substrate p - n grading factor FC Forward-bias depletion capacitor coefficient TF Ideal forward transit time NTF Transit-time bias dependence coefficient TF Transit-time dependency on V_{br} Transit-time dependency on I_r TR Ideal reverse transit time EG Bandgap voltage (barrier height) XTI(PT) IS temperature-effect exponent KF Ficker noise coefficient O.33 0.33 0.33 0.33 0.33 0.33 0.43 0.53 0.75 Farads 0.75 Volts 0.5 0.5 0.5 0.1NS 0.1NS 0.1NS Econds 0.1NS Econds 0.10NS Electron-volts 1.11 1.11 1.11 1.11	VJC(PC)		Base-collector built-in potential	Volts	0.75	0.75
XCJCFraction of C_{br} connected internal to R_B 1CJS(CCS)Collector-substrate zero-bias p - n capacitanceFarads0VJS(PS)Collector-substrate built-in potential0.75MJS(MS)Collector-substrate p - n grading factor0FCForward-bias depletion capacitor coefficient0.5TFIdeal forward transit timeSeconds0XTFTransit-time bias dependence coefficient0VTFTransit-time dependency on V_{br} Volts ∞ ITFTransit-time dependency on I_r Amps0PTFExcess phase at $1/(2\pi^*\text{TF})\text{Hz}$ Degrees030°TRIdeal reverse transit timeSeconds010NSEGBandgap voltage (barrier height)Electron-volts1.111.11XTBForward and reverse beta temperature coefficient3XTI(PT)IS temperature-effect exponent3KFFlicker noise coefficient06.6E-			Base-collector p-n grading factor	0.33	0.33	
CJS(CCS) Collector-substrate zero-bias p-n Farads VJS(PS) Collector-substrate built-in potential MJS(MS) Collector-substrate p-n grading factor FC FORWARD-bias depletion capacitor coefficient TF Ideal forward transit time Seconds VOIts Transit-time bias dependence coefficient TF Transit-time dependency on V _{bc} VTF Transit-time dependency on I _c PTF Excess phase at 1/(2π*TF)Hz TR Ideal reverse transit time EG Bandgap voltage (barrier height) XTB Forward and reverse beta temperature coefficient XTI(PT) IS temperature-effect exponent KF Flicker noise coefficient Volts Amps O JONS Electron-volts I.11 I.11 I.11 AGE O 6.6E-	XCJC		Fraction of C _{bc} connected internal		1	
tial MJS(MS) Collector-substrate p-n grading factor FC Forward-bias depletion capacitor coefficient TF Ideal forward transit time Seconds O O.1NS XTF Transit-time bias dependence coefficient TF Transit-time dependency on V _{bc} Volts TF Transit-time dependency on I _c Amps O PTF Excess phase at 1/(2n*TF)Hz TR Ideal reverse transit time Seconds O 10NS EG Bandgap voltage (barrier height) XTB Forward and reverse beta temperature coefficient XTI(PT) IS temperature-effect exponent KF Flicker noise coefficient	CJS(CCS)		Collector-substrate zero-bias p-n	Farads	0	2PF
MJS(MS) Collector-substrate p-n grading factor FC FC Forward-bias depletion capacitor coefficient IF Ideal forward transit time Seconds Transit-time bias dependence coefficient VTF Transit-time dependency on V _{bc} Volts TF Transit-time dependency on I _c Amps PTF Excess phase at 1/(2π*TF)Hz TR Ideal reverse transit time EG Bandgap voltage (barrier height) XTB Forward and reverse beta temper- ature coefficient XTI(PT) IS temperature-effect exponent KF Flicker noise coefficient 0 0.1NS Amps 0 Degrees 0 30° Electron-volts 1.11 1.11 1.11	VJS(PS)			Volts	0.75	
FC Forward-bias depletion capacitor coefficient IF Ideal forward transit time Seconds 0 0.1NS XTF Transit-time bias dependence coefficient VTF Transit-time dependency on V _{bc} Volts	MJS(MS)		Collector-substrate p-n grading		0	
TF Ideal forward transit time Seconds 0 0.1NS XTF Transit-time bias dependence coefficient VTF Transit-time dependency on V_{bc} Volts \approx ITF Transit-time dependency on I_c Amps 0 PTF Excess phase at $1/(2\pi^*TF)Hz$ Degrees 0 30° TR Ideal reverse transit time Seconds 0 10NS EG Bandgap voltage (barrier height) Electron-volts 1.11 1.11 XTB Forward and reverse beta temperature coefficient XTI(PT) IS temperature-effect exponent KF Flicker noise coefficient 0 6.6E-	FC		Forward-bias depletion capacitor		0.5	
XTF Transit-time bias dependence coefficient VTF Transit-time dependency on V_{bc} Volts \approx ITF Transit-time dependency on I_c Amps 0 PTF Excess phase at $1/(2\pi^*\text{TF})\text{Hz}$ Degrees 0 30° TR Ideal reverse transit time Seconds 0 10NS EG Bandgap voltage (barrier height) Electron-volts 1.11 1.11 XTB Forward and reverse beta temperature coefficient XTI(PT) IS temperature-effect exponent KF Flicker noise coefficient 0 6.6E-	TF			Seconds	0	0.1NS
VTFTransit-time dependency on V_{bc} Volts ∞ ITFTransit-time dependency on I_c Amps0PTFExcess phase at $1/(2\pi^{\circ}\text{TF})\text{Hz}$ Degrees030°TRIdeal reverse transit timeSeconds010NSEGBandgap voltage (barrier height)Electron-volts1.111.11XTBForward and reverse beta temperature coefficient03XTI(PT)IS temperature-effect exponent3KFFlicker noise coefficient06.6E-	XTF .		Transit-time bias dependence		0 .	
Transit-time dependency on I. Amps 0 PTF Excess phase at 1/(2\pi^*TF)Hz Degrees 0 30° TR Ideal reverse transit time Seconds 0 10NS EG Bandgap voltage (barrier height) Electron-volts 1.11 1.11 XTB Forward and reverse beta temperature coefficient XTI(PT) IS temperature-effect exponent KF Flicker noise coefficient 0 6.6E-	VTF			Volts	œ	
PTF Excess phase at 1/(2π*TF)Hz Degrees 0 30° TR Ideal reverse transit time Seconds 0 10NS EG Bandgap voltage (barrier height) XTB Forward and reverse beta temperature coefficient XTI(PT) IS temperature-effect exponent KF Flicker noise coefficient 0 6.6E-			Transit-time dependency on L.		0	
TR Ideal reverse transit time Seconds 0 10NS EG Bandgap voltage (barrier height) Electron-volts 1.11 1.11 XTB Forward and reverse beta temperature coefficient XTI(PT) IS temperature-effect exponent			Excess phase at 1/(2\pi*TF)Hz			30°
EG Bandgap voltage (barrier height) Electron-volts 1.11 1.11 XTB Forward and reverse beta temper- ature coefficient XTI(PT) IS temperature-effect exponent 3 KF Flicker noise coefficient 0 6.6E-						
XTB Forward and reverse beta temper- ature coefficient XTI(PT) IS temperature-effect exponent KF Flicker noise coefficient 0 6.6E-					-	
XTI(PT) IS temperature-effect exponent 3 KF Flicker noise coefficient 0 6.6E-	XTB		Forward and reverse beta temper-			-
KF Flicker noise coefficient 0 6.6E-	XTI(PT)				3	
I here hold bothers.			Flicker noise coefficient			6.6E-
A P PROKET HOUSE EXPONENT 1 1	AF		Flicker noise exponent		1	1

BJT MODEL PARAMETERS

MODEL

PARAMETER	CDIDODAM	SD1563BB	SD1563CC	SD1563DD	SD1563EE .
•	NPN	NPN	NPN	NPN	NPN
IS	1.000000E-06	5.000000E-06	10.000000E-06	50.00000E-06	100.000000E-06
BF	10	20	40	75	100.00000002-06
NF	1	1	1	1	100
VAF	10	50	100	150	300
IKF	2	10	20	30	200
ISE	100.00000E-09	500.000000E-09	1.000000E-06	5.00000E-06	40
NE	1.259	1.259	1.259	1.259	10.000000E-06
BR	. 1	.5	1	1.255	1.259
NR	1	1	1	1	4
IKR	ī	5	10	20	10
RB	.1	.125	.15	.175	10
RBM	.1	.125	.15	.175	.2
RE	.1	.125	15	.175	.2
RC	1.6	1.8	2	2.2	2.4
CJE	500.000000E-12	750.000000E-12	1.063000E-09	1.500000E-09	2.4
MJE	.2593	.2593	.2593	.2593	2.000000E-09
CJC	50.00000E-12	75.000000E-12	103.000000E-12	150.000000E-12	.2593
MJC	.3085	.3085	.3085	.3085	200.000000E-12
TF	2.000000E-12	4.000000E-12	6.000000E-12	8.000000E-12	.3085
XTF	2	2	2	2	10.00000E-12
VTF	4	4	4	4	2
ITF	. 4	. 4	- - 4	- A	4
TR	100.00000E-12	400.000000E-12	600.00000E-12	800.000000E-12	.4
XTB	1.5	1.5	1.5	1.5	1.000000E-09 1.5

VOLTAGE SOURCE CURRENTS NAME CURRENT

V_V1 3.315E+01 V_V2 -3.216E+01

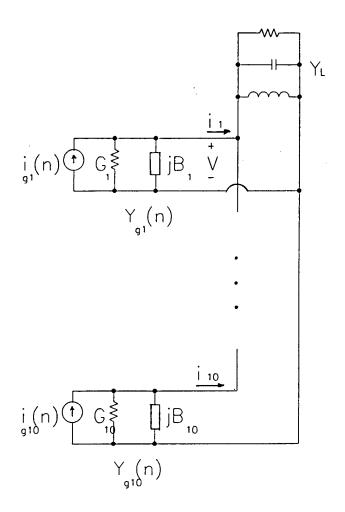
TOTAL POWER DISSIPATION 1.55E+03 WATTS

SUMMARY

Mismatched transistors can be paralleled in a UHF power amplifier with no noticeable degradation in performance.

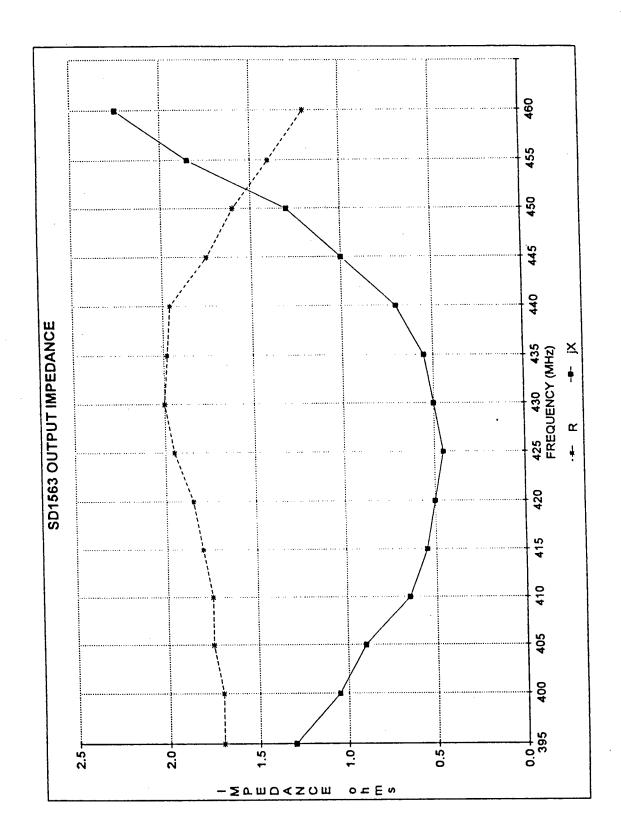
UHF POWER AMPLIFIER NETWORK SIMULATION

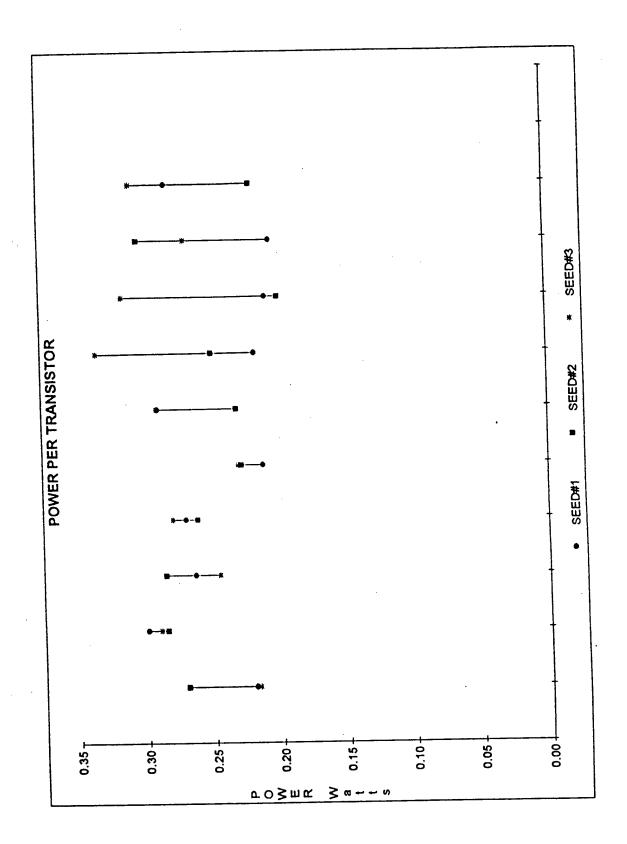
Objective: Examine the effect of conjugate matching with paralleled mismatched transistors.

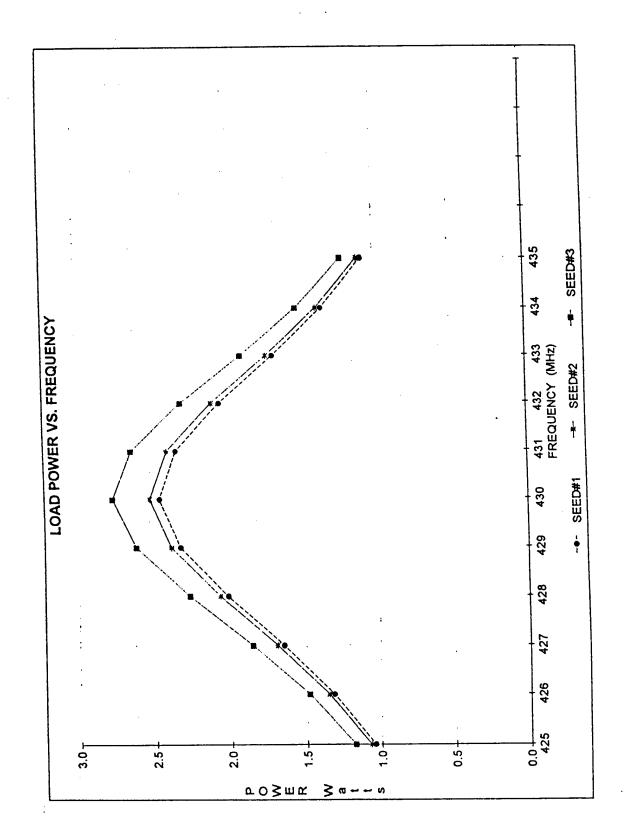


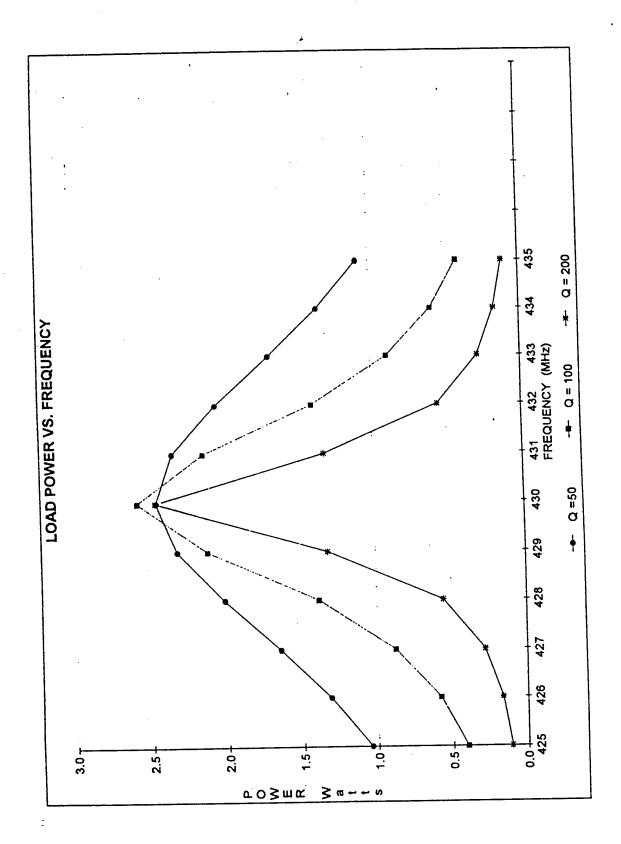
$$Y_L = \left(\sum_{i=1}^{i=10} Y_{gi}\right)^*$$
 at resonance

Re (i gi), Im(i gi), G , B are all perturbed $\pm -10\%$ around nominal values using a random number generator



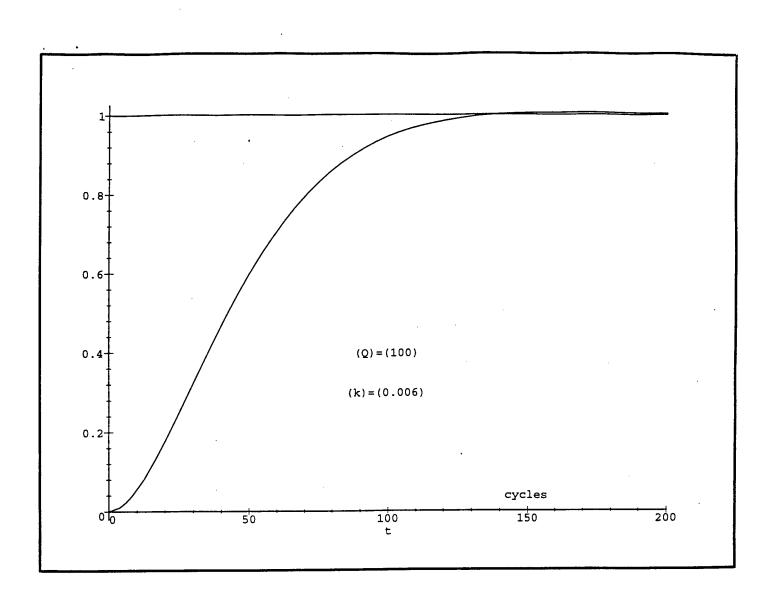


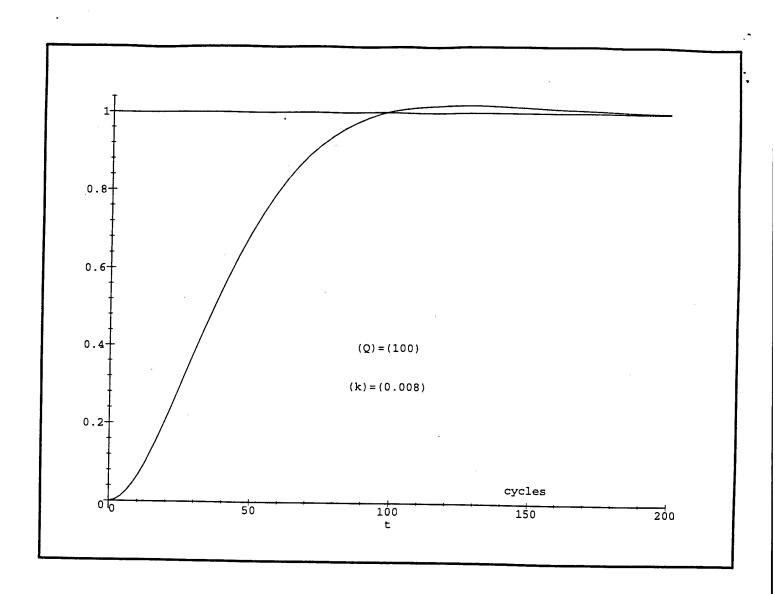


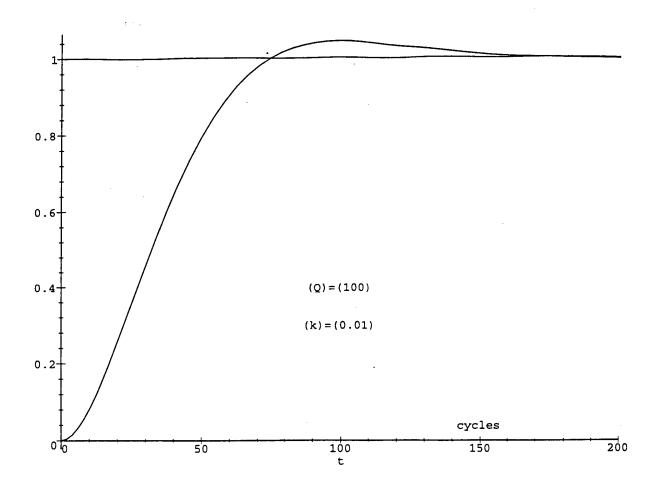


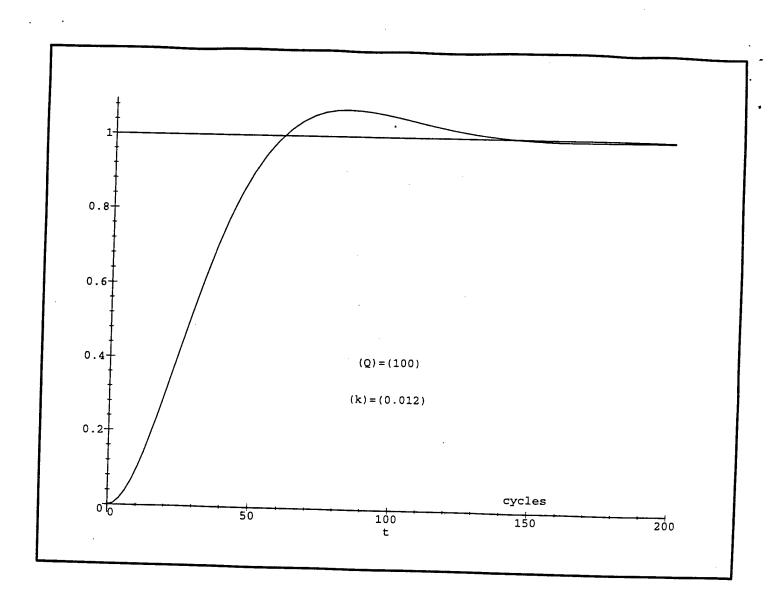
SUMMARY

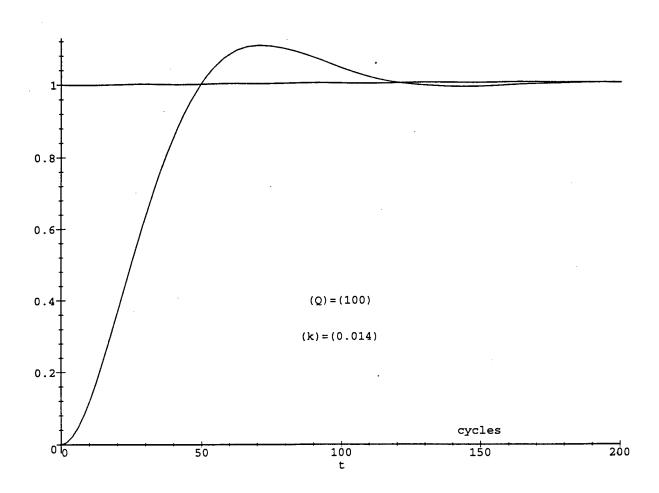
Conjugate matching the load admittance to the sum of the parallel transistor output admittances yields good steady state ac amplifier performance even for the case of mismatched transistors.

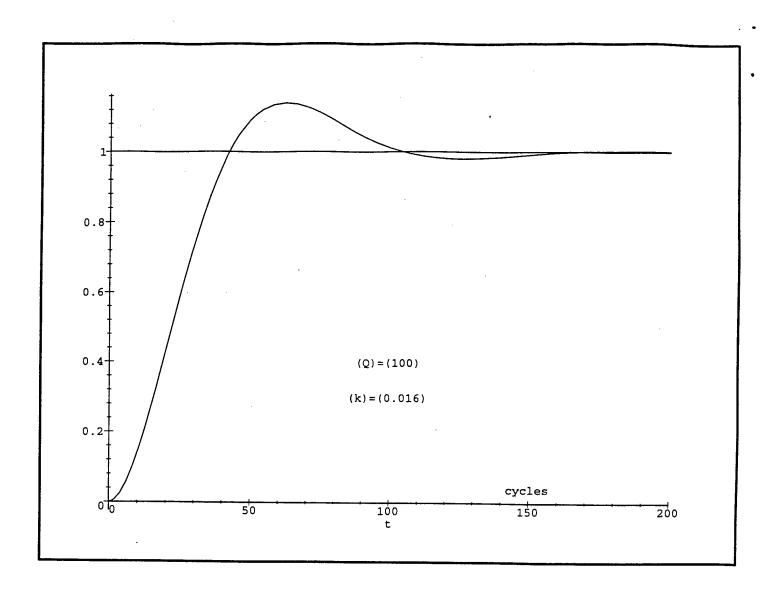












 $> f:=x->x^4/((x-i)^*(x+i)^*(x+q-i-a^*i)^*(x+q+i+a^*i)^*(x+q-i+a^*i)^*(x+q+i-a^*i));$

$$f := x \to x^4 / ((x-I)(x+I)(x+q-I-Ia)(x+q+I+Ia))$$
$$(x+q-I+Ia)(x+q+I-Ia))$$

> readlib(residue);

proc(f,a) ... end

> r0:=residue(f(x),x=l);

$$r0 := -\frac{1}{2} \frac{I}{(-q+Ia)(2I+q+Ia)(q+Ia)(-2I-q+Ia)}$$

> r1:=residue(f(x),x=-q+l+a*l);

$$rl := -\frac{1}{4} \frac{(-q+I+Ia)^4}{(-q+Ia)(-q+2I+Ia)(2I+2Ia)a}$$

> r2:=residue(f(x),x=-q+l-a*l);

$$r2 := -\frac{1}{4} \frac{(q - I + Ia)^4}{(q + Ia)(q - 2I + Ia)a(-2I + 2Ia)}$$

> r0m:=(Re(r0)^2+lm(r0)^2)^.5;

$$r0m := \left(\frac{1}{4}\Im\left(\frac{1}{(-q+Ia)(2I+q+Ia)(q+Ia)(-2I-q+Ia)}\right)^{2} + \frac{1}{4}\right)$$

$$\Re\left(\frac{1}{(-q+Ia)(2I+q+Ia)(q+Ia)(-2I-q+Ia)}\right)^{2}\right)^{5}$$

> rr:=r0/r0m;

$$rr := -\frac{1}{2}I / \left((-q + Ia) (2I + q + Ia) (q + Ia) (-2I - q + Ia) \right)$$

$$\frac{1}{4} \Im \left(\frac{1}{(-q + Ia) (2I + q + Ia) (q + Ia) (-2I - q + Ia)} \right)^{2}$$

$$+ \frac{1}{4}$$

$$\Re \left(\frac{1}{(-q + Ia) (2I + q + Ia) (q + Ia) (-2I - q + Ia)} \right)^{5} \right)$$

> rp:=(r1+r2)/r0m;

$$rp := \left(-\frac{1}{4} \frac{(-q+Ia)(-q+2I+Ia)^4}{(-q+Ia)(-q+2I+Ia)(2I+2Ia)a} - \frac{1}{4} \frac{(q-I+Ia)^4}{(q+Ia)(q-2I+Ia)a(-2I+2Ia)} \right) / \left(\frac{1}{4} \Im \left(\frac{1}{(-q+Ia)(2I+q+Ia)(q+Ia)(-2I-q+Ia)} \right)^2 + \frac{1}{4} \right)$$

$$\Re\left(\frac{1}{(-q+Ia)(2I+q+Ia)(q+Ia)(-2I-q+Ia)}\right)^{2})^{5}$$

$$> rm:=(r1-r2)/r0m;$$

$$rm := \left(-\frac{1}{4} \frac{(-q+Ia)(-q+2I+Ia)^{4}}{(-q+Ia)(-q+2I+Ia)(2I+2Ia)a} + \frac{1}{4} \frac{(q-I+Ia)^{4}}{(q+Ia)(q-2I+Ia)a(-2I+2Ia)}\right) / \left(\frac{1}{4} \Im\left(\frac{1}{(-q+Ia)(2I+q+Ia)(q+Ia)(-2I-q+Ia)}\right)^{2} + \frac{1}{4} \right)$$

$$\Re\left(\frac{1}{(-q+Ia)(2I+q+Ia)(q+Ia)(-2I-q+Ia)}\right)^{2})^{5}$$

$$> a:=.006;$$

$$a:=.006$$

$$> q:=.005;$$

$$rr;$$

$$-.005000013645 + .9999874995 I$$

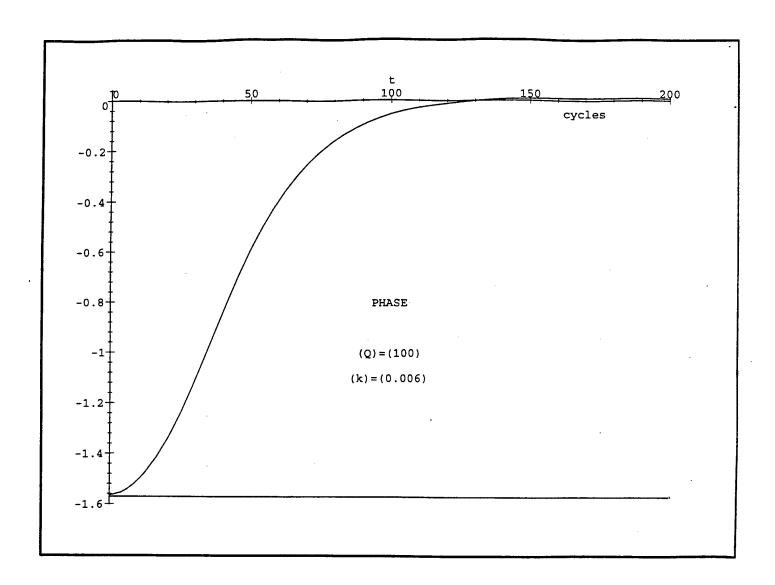
$$> rr;$$

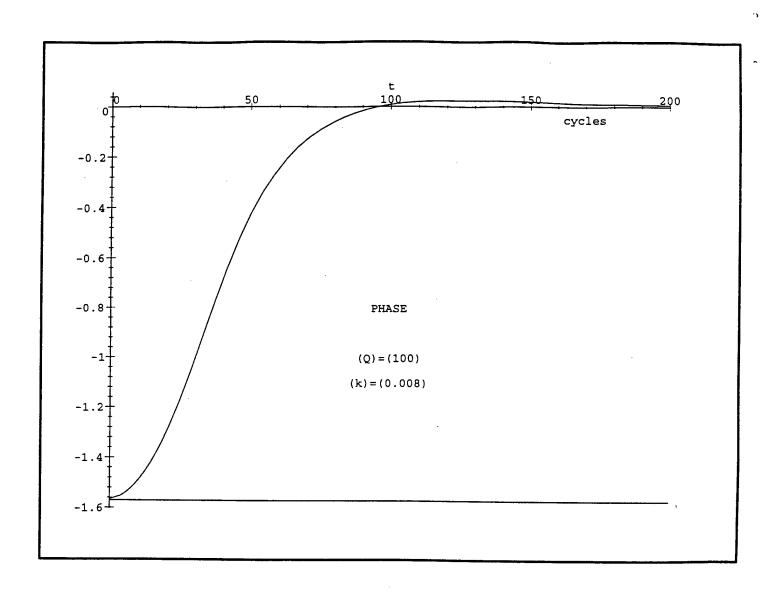
$$-.005000013755 - 1.000079002 I$$

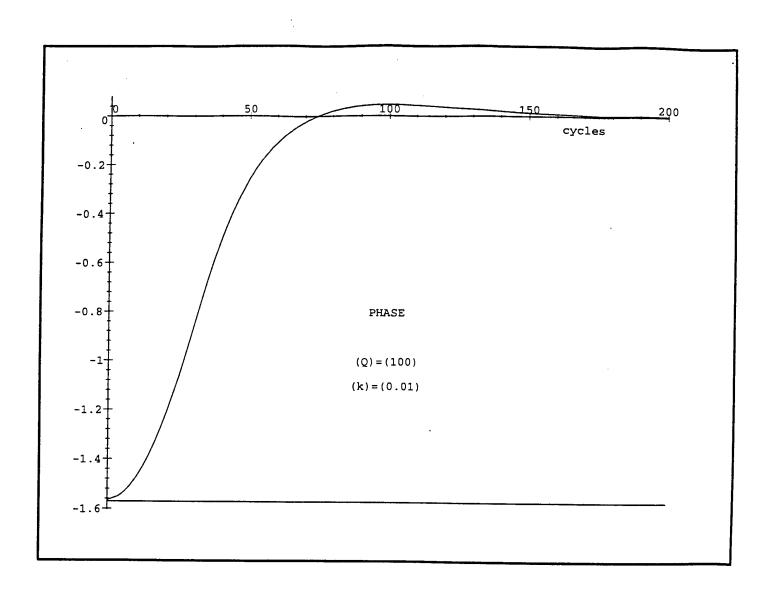
$$> rm;$$

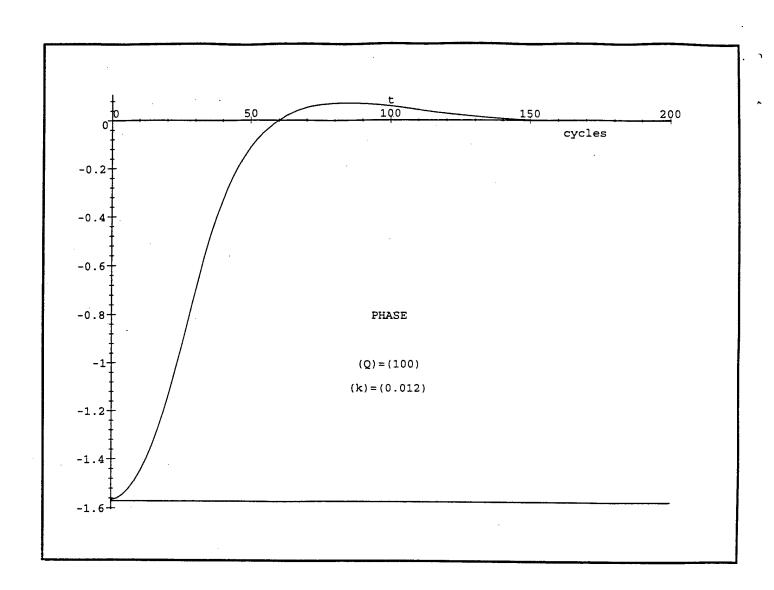
-.8331450010 - .02958297129 *I*

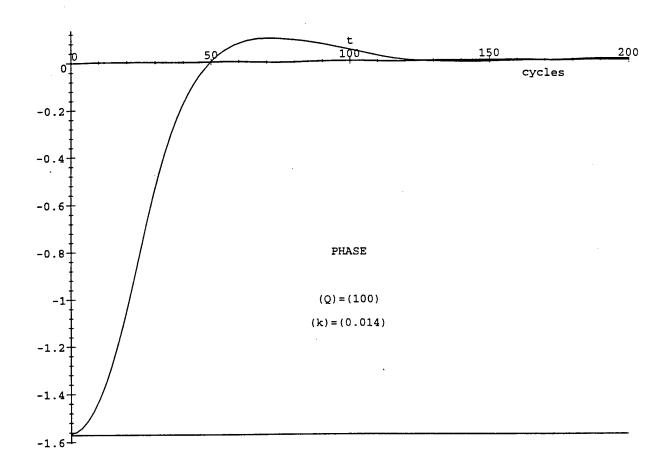
```
> a0r:=Re(rr);
                            a0r := -.005000013645
 > a0i:=lm(rr);
                               a0i := .9999874995
> apr:=Re(rp);
                             apr := .005000013755
> api:=lm(rp);
                              api := -1.000079002
> amr:=Re(rm);
                             amr := -.8331450010
> ami:=lm(rm);
                            ami := -.02958297129
> hc:=t->a0r+exp(-2*Pi*q*t)*(apr*cos(2*Pi*a*t)-ami*sin(2*Pi*a*t));
   hc := t \rightarrow a0r + e^{(-2\pi q t)} \left( apr \cos(2\pi a t) - ami \sin(2\pi a t) \right)
> hs:=t->-a0i-exp(-2*Pi*q*t)*(api*cos(2*Pi*a*t)+amr*sin(2*Pi*a*t));
  hs := t \rightarrow -a0i - e^{(-2\pi q t)} (api \cos(2\pi a t) + amr \sin(2\pi a t))
h:=t->(hc(t)^2+hs(t)^2)^.5;
                         h := t \to \left( \operatorname{hc}(t)^2 + \operatorname{hs}(t)^2 \right)^{.5}
> with(plots,textplot,display);
                               [display, textplot]
> P:=plot(\{h(t),1\},t=0..200):
> R:=textplot({[100,.4,'Q=100'],[100,.3,'k=.012'],[150,.04,'cycles']}):
> display({P,R});
```

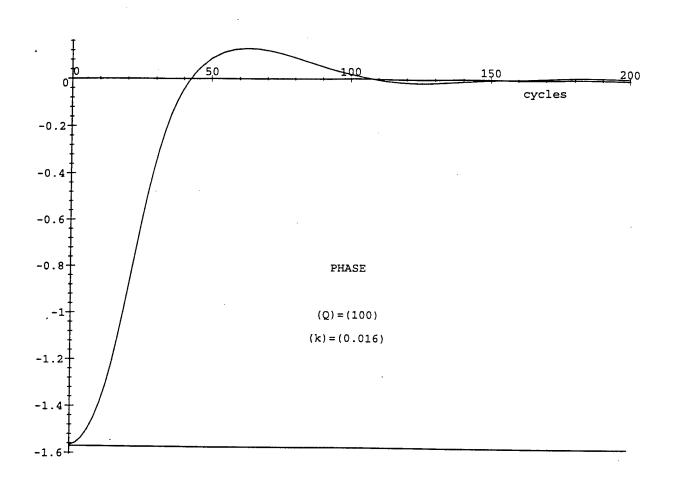


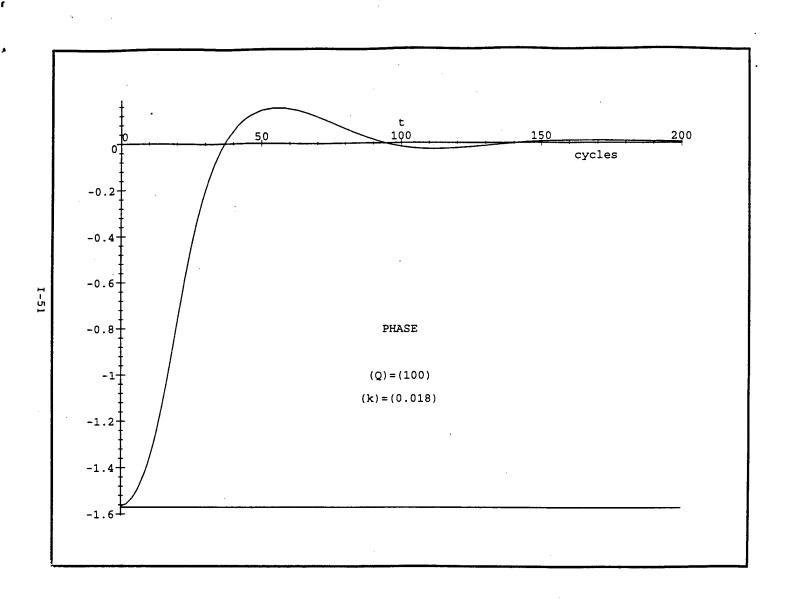












 $> f:=x->(x^4-x^3)/((x-i)^*(x+i)^*(x+q-i-a^*i)^*(x+q+i+a^*i)^*(x+q-i+a^*i)^*(x+q+i-a^*i));$

$$f := x \to (x^4 - x^3) / ((x - I)(x + I)(x + q - I - Ia))$$

$$(x + q + I + Ia)(x + q - I + Ia)(x + q + I - Ia))$$

> readlib(residue);

proc(f,a) ... end

> r0:=residue(f(x),x=l);

$$r0 := \frac{\frac{1}{2} - \frac{1}{2}I}{(q - Ia)(2I + q + Ia)(q + Ia)(2I + q - Ia)}$$

> r1:=residue(f(x),x=-q+l+a*l);

$$rI := -\frac{1}{4} \frac{(-q+I+Ia)^3 (-1-q+I+Ia)}{(-q+Ia) (-q+2I+Ia) (2I+2Ia) a}$$

> r2:=residue(f(x),x=-q+l-a*l);

$$r2 := \frac{1}{4} \frac{(-q+I-Ia)^3 (-1-q+I-Ia)}{(-q-Ia) (-q+2I-Ia) a (2I-2Ia)}$$

> r0m:=(Re(r0)^2+lm(r0)^2)^.5;

$$r0m := \left(\Re\left(\frac{\frac{1}{2} - \frac{1}{2}I}{(q - Ia)(2I + q + Ia)(q + Ia)(2I + q - Ia)}\right)\right)$$

$$+ \Im \left(\frac{\frac{1}{2} - \frac{1}{2}I}{(q - Ia)(2I + q + Ia)(q + Ia)(2I + q - Ia)} \right)^{2} \right)^{5}$$

> rr:=r0/r0m:

$$rr := \left(\frac{1}{2} - \frac{1}{2}I\right) / \left((q - Ia)(2I + q + Ia)(q + Ia)\right)$$

$$(2I + q - Ia) \left(\frac{1}{2} - \frac{1}{2}I\right)$$

$$\Re \left(\frac{\frac{1}{2} - \frac{1}{2}I}{(q - Ia)(2I + q + Ia)(q + Ia)(2I + q - Ia)}\right)^{2}$$

$$+ \Im \left(\frac{\frac{1}{2} - \frac{1}{2}I}{(q - Ia)(2I + q + Ia)(q + Ia)(2I + q - Ia)}\right)^{2}\right)^{5}$$

$$rp := \left(-\frac{1}{4} \frac{(-q + I + Ia)^{3}(-1 - q + I + Ia)}{(-q + Ia)(-q + 2I + Ia)(2I + 2Ia)a}\right)^{6}$$

$$+\frac{1}{4} \frac{(-q+I-Ia)^{3}(-1-q+I-Ia)}{(-q-Ia)(-q+2I-Ia)a(2I-2Ia)} \bigg) \bigg/ \bigg($$

$$\Re \left(\frac{\frac{1}{2} - \frac{1}{2}I}{(q-Ia)(2I+q+Ia)(q+Ia)(2I+q-Ia)} \right) \bigg) \bigg|$$

$$\sqrt{(q-Ia)(2I+q+Ia)(q+Ia)(2I+q-Ia)}$$

$$+\Im\left(\frac{\frac{1}{2} - \frac{1}{2}I}{(q - Ia)(2I + q + Ia)(q + Ia)(2I + q - Ia)}\right)^{2}\right)^{5}$$
r1-r2)/r0m;

$$rm := \left(-\frac{1}{4} \frac{\left(-q + I + Ia \right)^{3} \left(-1 - q + I + Ia \right)}{\left(-q + Ia \right) \left(-q + 2I + Ia \right) \left(2I + 2Ia \right) a} \right.$$

$$\left. -\frac{1}{4} \frac{\left(-q + I - Ia \right)^{3} \left(-1 - q + I - Ia \right)}{\left(-q - Ia \right) \left(-q + 2I - Ia \right) a \left(2I - 2Ia \right)} \right) \middle/ \left(\frac{1}{4} \right) \left. -\frac{1}{4} \left(-\frac{1}{4} \right) \left(-\frac{1}{4}$$

$$\Re\left(\frac{\frac{1}{2} - \frac{1}{2}I}{(q - Ia)(2I + q + Ia)(q + Ia)(2I + q - Ia)}\right)^{2}$$

$$+\Im\left(\frac{\frac{1}{2} - \frac{1}{2}I}{(q - Ia)(2I + q + Ia)(q + Ia)(2I + q - Ia)}\right)^{2}\right)^{5}$$

> a:=.009;

a := .009

> q:=.005;

q := .005

> rr;

-.7106335256 + .7035623584 I

> rp;

.7106335258 - .7036751639 *I*

> rm; -.3782301986 - .4155746343 *I* > a0r:=Re(rr); a0r := -.7106335256> a0i:=lm(rr); a0i := .7035623584> apr:=Re(rp); apr := .7106335258> api:=lm(rp); api := -.7036751639> amr:=Re(rm); amr := -.3782301986> ami:=lm(rm); ami := -.4155746343> hc:=t->.5*(a0r+a0i)+exp(-2*Pi*q*t)*(apr*cos(2*Pi*a*t)-ami*sin(2*Pi*a*t)); $hc := t \rightarrow .5 \ a0r + .5 \ a0i$ $+ \operatorname{e}^{(-2\pi q\,t)} \left(apr\cos(2\pi a\,t) - ami\sin(2\pi a\,t) \right)$ > hs:=t->.5*(a0r-a0i)-exp(-2*Pi*q*t)*(api*cos(2*Pi*a*t)+amr*sin(2*Pi*a*t)); $hs := t \rightarrow .5 \ a0r - .5 \ a0i$ $-e^{(-2\pi q t)}(api\cos(2\pi a t) + amr\sin(2\pi a t))$ > h:=t->arctan(hc(t)/hs(t)); $h := t \rightarrow \arctan$ > with(plots,textplot,display);

[display, textplot]

> P:=plot({h(t),-Pi/2},t=0..200): > > R:=textplot({[100,-.8,'PHASE'],[100,-1,'Q=100'],[100,-1.1,'k=.018'],[170,-.05,'cycl_es']}):
> display({P,R});
>

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